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Standard Cell Design with Low Leakage Using Gate Length Biasing in Cadence Virtuoso and ALU Using Power Gating Sleep Transistor Technique in Soc Encounter

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***Abstract*—The leakage current, power and area have become import parameters incircuit designing as the technology is scaling.Leakage power has become one of the most critical design concerns for the system level chip designer. While lowered supplies and hence lowered threshold voltage) and aggressive clock gating can achieve dynamic power reduction, these techniques increase the leakage power and, therefore, causes its share of total power to increase. The basic gates such as inverter, NAND, and NOR are important elements in digital circuits.Gate length biasing is a method to optimize the design by varying the gate length so as to decrease power dissipation. In the current technology, the leakage power is the major contributor to the total power consumption . Power gating and clock gating are technique which are used to reduce the leakage power by switching off the unused transistors and clock using sleep transistor technique.**

***keywords*— standard cell, gate length, power dissipation, sleep transistor, power gating, clock gating, leakage power**

I.INTRODUCTION

Energy dissipation in CMOS designs is mainly of two type's .Its either static or dynamic. [1]. The dynamic energy dissipation includes switching energy due to charging and discharging of load capacitances, and short energy due to a direct-path from supply voltage to the ground. The short energy dissipation can usually be ignored. Static energy dissipation is caused by leakage currents of MOS devices. Leakage is become an ever-increasing components of total dissipated power with its contribution projected to increase from 18% at 130nm to 54% at 65nm node [2].Leakage is composed of three major components - subthreshold leakage , gate leakage , reverse-biased drain substrate and source-substrate junction band-to-band tunneling leakage [4]. Subthreshold leakage is the dominant contributor to the total leakage [4].

Although process scaling reduces the energy needed to perform a given computation since wires and transistors are smaller, it increases power dissipation per unit area and therefore the overall power for a given die size.

II. TECHNIQUES TO REDUCE THE POWER DISSIPATION IN CMOS CIRCUITS

A. Gate Length Biasing Of Standard Cell

Subthreshold leakage is the dominant contributor to totalleakage at 130nm and remains so in the future [4]. PDP (Power Delay Product) metric provides a good compromise between speed and delay, which is written as [1]

$$EDP=E\cdot t_{\text{delay}}$$

The basic gates such as inverter, NAND, and NOR are important elements in digital circuits. In this work , a two input Inverter is optimized using gate length biasing by varying gate length from 180nm to 250 nm.

B. Submicron Technique And Optimized Sleep Transistor

Micron is the measurement of length. Submicron technology allows billions of transistors on a single die, potentially running at GHz frequencies. Submicron condition is sub threshold condition.This method employs power gating.Power gating is one of

the techniques in circuits whichis used to reduce the leakage power by shutting off the idle logicblocks using sleep transistors. Different power gating methodsare available now.

These helps in reducing the power, delay andswitching time of the logics.This method enables the control logic to turn off selected components in design during the inactive state. The components are invoked again when any activity is detected. Power gating when combined with other techniques such as RBB can achieve more than 100 times less leakage power in sleep mode[7].

In this work, several basic standard cell inverter is simulated with different gate lengths and delay and power is calculated .All simulation are performed using Spectre in cadence and delay and power are calculated.Also a RTL-to-GDSII design of a 4 bit accumulator is generated using RTL synthesis NClaunch and SOC encounter.Then Sub micron technique is used to design a low leakage accumulator.Power gating is implemented.

III. GATE LENGTH BIASING METHODOLOGY

For short channel devices, with increasing of the gate length, the threshold voltage increases, so that the leakage decreases exponentially and delay increases linearly. The gate-length biasing (GLB) technology increases the channel length of transistors to alter the threshold voltage and reduces leakage exponentially in both active and standby modes, while delay increases linearly with increasing gate length [6].In this work atestcase is designed in cadence virtuoso 9.1 .The design is of two input inverter in 180nm .Spectre simulation is performed.Delay is calculated and leakagepoweriscalculated.

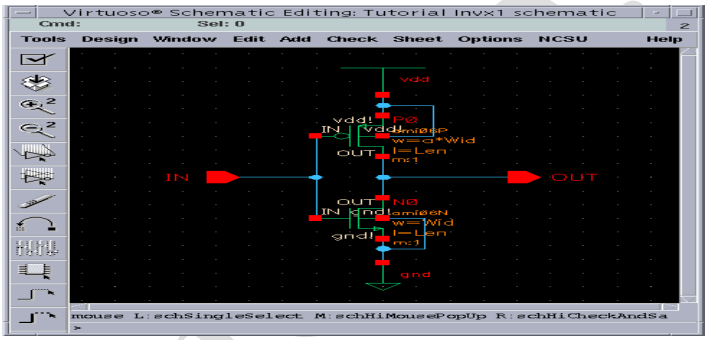

Fig1.Schematic of two input inverter in cadence virtuoso 9.1

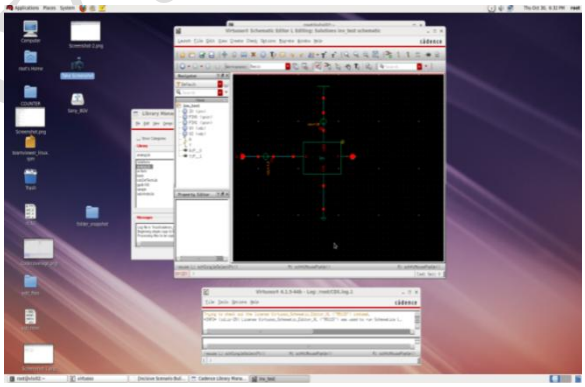

Fig2.Testcase of inverter in cadence.

Spectre simulation is performed in cadence.DC and Transient analysis are performed .

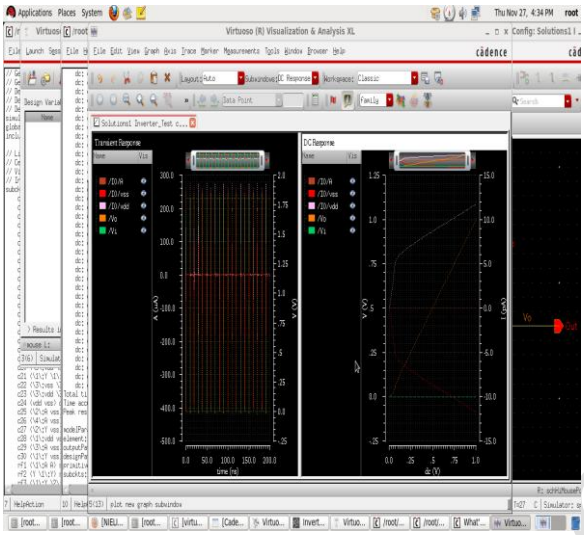

Fig3. DC and Transient analysis of inverter using spectre simulation

Next Delay and power dissipation is calculated.

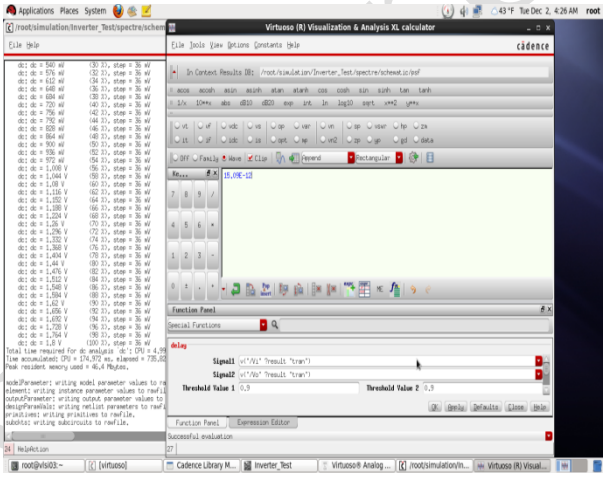

Fig 4.Delay calculation using virtuoso tool

Next , values of gate length of inverter cell are changed to bating different values of power dissipation and delay.

Following are the value of delay and power dissipation calculatedwhen gate length is varied from 180,200,250nm

TABLE.1.DELAY AND POWER DISSIPATION VALUE FOR DIFFERENT GATE LENGTH.

Gate length(nm)	Delay calculation(ps)	Power dissipated(pw)
180	13.65	61.7
200	15.09	59.7
250	18.89	50.8

Thus the value of Power dissipation decreases exponentially on increasing the gate length of design

As the gate length is increased we observe that leakage power decreases.This concept can be used to design circuits employing standard cells .By using gate length biased cells instead of normal standard cells.This is however at cost of increased delay. Hence optimized design is obtained.

IV.SUBMICRON TECHNIQUE AND OPTIMIZED SLEEP TRANSISTOR

During inactive states, the devices keep consuming certain power which is dominated by the leakage power consumption of all the components. The designers should provide a mechanism to reduce this leakage power consumption. We are considering the problem of reducing leakage power consumption of ALU by providing a Sleep Mode. Firstly a four bit ALU is designed using RTL synthesis, NClaunch and SOC encounter .The full RTL to GDS flow is performed to obtain the design.

RTL to GDS flow

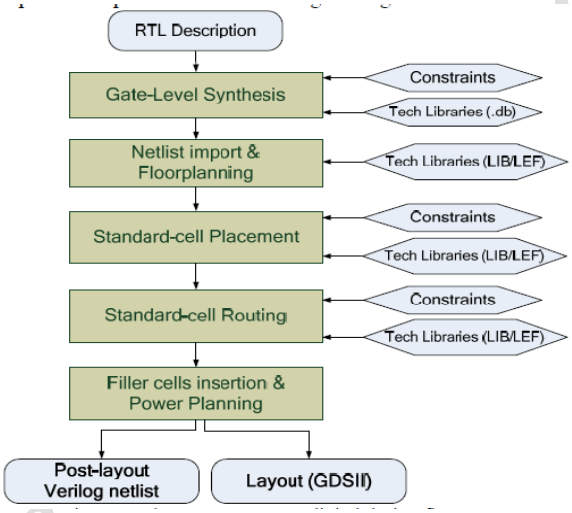

Fig 5. Flow diagram of complete RTL to GDS [5]

Leakage power is calculated is calculated as 13.757nW

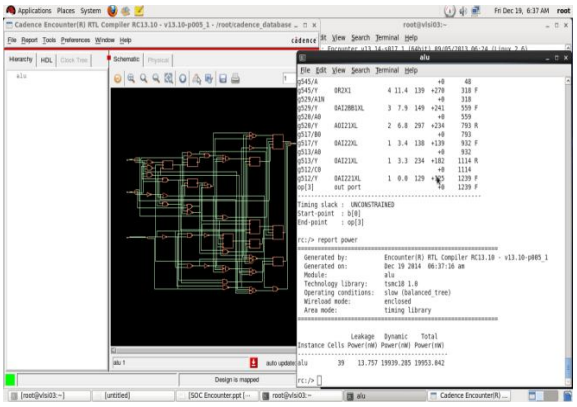

Fig 6. Leakage power calculation of 4 bit ALU design .

Floorplanning andRouting of design are performed in SOC Encounter .

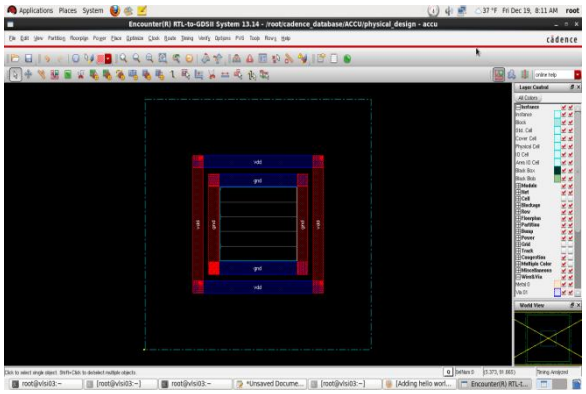

Fig 7.floorplanning and power planning of alu

Thus ALU is designed as shown in figure 8.

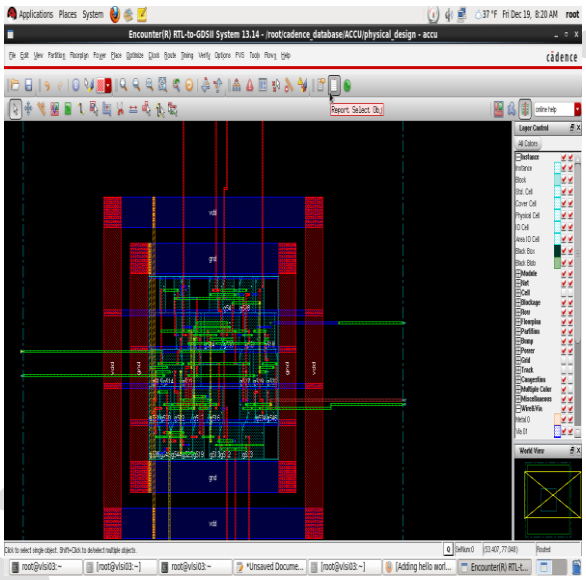

Fig 8.Complete design of ALU in SOC encounter

V.SLEEP MODE POWER GATING

Power-gating technique or sleep mode sub micron technique uses a high Vth sleep transistor in series with the pull-up and/or the pull-down of a low Vth logic block to reduce leakage power. The sleep transistor can be turned off when the low Vth logic block is inactive, thus resulting in a significant reduction of sub-threshold leakage current.A sleep transistor can be a high Vth NMOS or PMOS transistor [7]. A PMOS sleep transistor served as a header switch connects the power network to virtual VDD. An NMOS sleep transistor served as a footer switch connects the ground network to virtual GND. Normally, either a header switch or a footer switch is used to conserve area and reduce timing penalty caused by voltage drop across sleep transistors.

The sleep transistors can be implemented in 2 ways called as Header and Footer types as shown in Figure 8. Though both the types achieve the power gating, they have their pros and cons. We discuss these in this section.

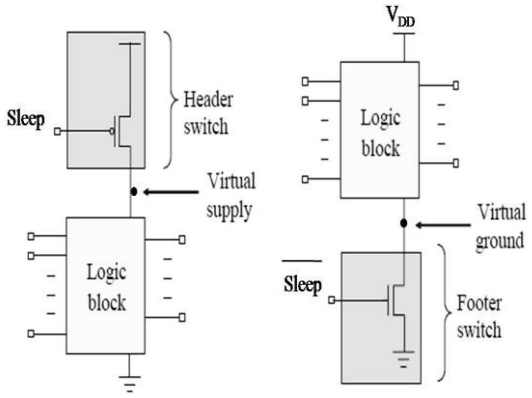

Fig 9. Sleep transistor implementation using Header and footer methodology[7].

The header switch is implemented by PMOS transistors to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of a same size. The NBTI effect increases Vth over time and makes PMOS transistor even less leaky. Header switches turn off VDD and keep VSS on. As the result, it allows a simple design of a pull-down transistor to isolate power-off cells and clamp output signals in "0" state. The "0" state isolation is complied with reset state requirement in most designs. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size, though difference is reduced by strained silicon technology. As a result, a header switch implementation usually consumes more area than a footer switch implementation.

The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area. However, NMOS is leakier than PMOS and application designs become more sensitive to ground noise on the virtual ground (VVSS) coupled through the footer switch. The isolation on "0" state becomes complex due to loss of the virtual ground in sleep mode and necessity of bypassing footer switch to reach permanent VSS. In the following part of the paper, we shall focus on header switch design and implementations.

This work has many transistors to use in the sleep transistor network so considering the area penalty; it is decided to use a footer type of transistor structure.

Also some other design decisions made are discussed here. A Local sleep transistor network is used as opposed to Global or cell level transistors. As the gate count of original circuit is about 1450, a cell based design would require equal number of sleep transistors which is a high area overhead. As this circuit is a pure combinational logic, no data retention technique has been used. The output of a power gated circuit needs to be isolated from the next stage of logic as the crowbar currents may create excessive power consumption in next stage. This is done by using a simple circuits like a isolation cells made by AND or OR. Also, clamped pull-up or pull-down transistors can be used. A level shifter approach is also discussed in [7]. The ALU circuit under experimentation is an isolated block with buffers at SUM output to provide output capacitances so we have not implemented the current isolation circuit.

One of the most critical decisions in power gating is the design of Sleep Transistor. In this work we have considered a worst case scenario of current through the sleep transistor as a design criterion. The Sleep transistor resistance should be large enough in sleep mode to produce a considerable voltage drop, almost equal to VDD, between GND and Virtual GND. Also the on resistance should be as small as possible as it will have the least effect on discharge path delay and hence on the speed of the circuit. But these requirements always contradict each other because a smaller resistance means wider area of transistor which causes more power consumption so there is always a tradeoff between leakage power saving and speed of the circuit.

Considering above worst case current scenario, a Sleep transistor is designed as follows.

Delay of a single gate without sleep mode is given as [7]

$$\tau d = \frac{C_L V_{DD}}{(V_{DD} - V_{tL})^{\alpha}} \ldots\ldots (1)$$

Where, VDD is the supply voltage, VtL is low level threshold voltages, α is Saturation Velocity Index and CL is the load capacitance.

If a sleep transistor of High Vt is introduced, we get delay as

$$\tau d^{Sleep} = \frac{C_L V_{DD}}{(V_{DD} - Vx - V_{tL})^{\alpha}} \quad \ldots\ldots (2)$$

Where, Vx is the drop across sleep transistor while the circuit is in active mode

Allowing 5% overhead in the delay for this design, we get

$$\frac{\tau d}{\tau d^{Sleep}} = 95\% \quad \ldots\ldots (3)$$

Solving this equation for α=1.8 gives, the voltage drop across sleep transistor as $Vx = 0.0281(V_{DD} - V_{tL})$ ……. (4)

The current through the sleep transistor is represented approximately by

$$I_{Sleep} \approx \mu_n C_{ox} \left(\frac{W}{L}\right)_{Sleep} (V_{DD} - V_{tL})(V_{DD} - V_{tH}) \quad \ldots\ldots (5)$$

Where, μn is mobility of electrons = 150 cm2/V.s at 90oC, Cox is oxide capacitance = 19.7 X 10-6 F/m for 45nm [7].

So the width over length ratio of a sleep transistor is given by

$$\left(\frac{W}{L}\right)_{Sleep} = \frac{I_{Sleep}}{0.0281\mu_n C_{ox}(V_{DD} - V_{tL})(V_{DD} - V_{tH})} \quad \ldots\ldots (6)$$

Isleep is calculated by simulating the ALU circuit without sleep transistor network and finding maximum current that flows through ground.

VI.CONCLUSION AND FUTURE WORKS

We can see that gate length biasing is an effective method to reduce the power dissipation . As gate length is increased from 180nm to 250 nm, the paw dissipated decreases exponentially and delay increases linearly.Thus design is optimized . Also a complete RTL to GDS flow of a Accumulator is performed in SOC encounter.We can also see that Power gating sleep mode transistor technique is an effective technique to reduce leakage power consumption of a combinational logic block like ALU during inactive state. Savings can be as much as 99% of the total power consumption with only proper sleep transistor network. The switching currents/ fluctuations can be further reduced by applying a constant low leakage vector at the input of the circuit during sleep mode.In future we can apply this power gating technique to other combinational and sequential blocks like PLA ,ROM ,RAM etc. Also the area overhead is quite high which can be reduced with selective clustering of transistors in the ALU as a part of future work.

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