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International Journal of Innovative Research in Technology, Science & Engineering (IJIRTSE)
ISSN: 2395-5619, Volume – 1, Issue – 2. April 2015

FPGA-BASED DATA ACQUISITION SYSTEM WITH RS 232 INTERFACE

[1]Thirunavukkarasu.T, [2]Kirthika.N
[1]PG Student: Department of ECE (PG), Sri Ramakrishna Engineering College, Coimbatore, India
[2]Assistant Professor, Department of ECE (PG), Sri Ramakrishna Engineering College, Coimbatore, India
[1]arasu455@gmail.com, [2]Kirthika.natarajan@srec.ac

***Abstract*— This describes implementation of data acquisition system on FPGA.FPGA works as a data acquisition system and transfers data from the ADC to the output device. At the end of data acquisition, the FPGA data can be transmitted to the PC through the RS 232 interface .The system is controlled by software written in the visual C++. It allows the user to be able to interface to a PC for data restoration and monitoring..All modules were designed in VHDL& simulated using Xilinx-ISE 12.3 and Xilinx Spartan -3E.**

***Keywords*— FPGA, ADC, Xilinx, and Spartan-3E kit**

I. INTRODUCTION

The data acquisition systems are widely used as automatic test and measuring equipments in many industries. It can be used to collect the data from number of peripheral input devices, such as meters, sensors and etc.The measured data could be stored in the personal computer through controlling software. The values can be displayed numerically and their relationship can be displayed graphically on the screen. Data acquisition system is mainly depends on bus is used in it. Buses are main part of data transmission between the electronic devices. The aim of implementing bus is used to collect the data from sensors or analog to digital converters.

This paper proposed a design of the data acquisition system using FPGA interfacing to a PC. The system has capability to receive the digital signals from sensors with parallel ADC protocols. Parallel protocol implanted on FPGA kit and modeled using VHDL.

II. OVERALL SYSTEM

The overall system is shown in Fig 1. It presents the connection to the ADC (analog to digital converter) with parallel protocol. The FPGA collects the individual data from ADC. It processes in the ADC protocols. At the end it produces a stream of data through the output UART port, which sends these ADC data to the PC. We have written a specific application software program to control the PC. This program has a responsibility to communicate to the FPGA so that the PC could prepare itself for the data transfer. Firstly, the PC will check the FPGA for data availability on the system. After that it will send a set of the instructions to the FPGA for getting these data from UART port. The data will be interpreted into separate data bytes for the individual channels. Finally, the data can be shown to the user, and saved to the main database at the same time.

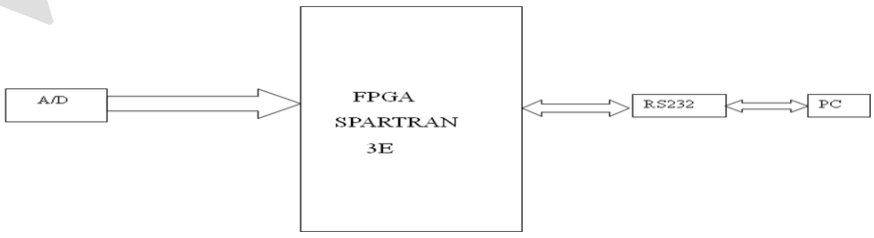

Fig -1: Overall system diagram

The System would process parallel protocols and produce data at the output. Which intern connected to the PC to visualize the output waveform.

III. Device Selection

A. FPGA Selection

The processing unit SPARTAN-3E from Xilinx Company is employed for this design. It has 2160 capacity logic elements or about 100,000 gates, Four 18K-bit block RAMs (72K bits) and 3 numbers of 8 pin header to interface VLSI based experiment modules. It supports the power supply at 2 levels, which are 5V, 3.3V. The maximum on board operating frequency is 24 MHz. This design has used VHDL as the language for writing the code program. This kit works as the center of the acquisition of the data from ADC. Its responsibility is to bridge the signals between the ADC inputs to the RS232 connection namely, to send/receive the data with the PC.

B. ADC Selection

ADC0804 is a very commonly used 8-bit analog to digital convertor. It is a single channel IC so can take only one analog signal as input. Since it is 8 bit ADC the digital outputs varies from 0 to a maximum of 255. By setting the reference voltage at pin9 the step size can be adjusted. When this pin is not connected, the reference voltage is the operating voltage(VCC)

ADC0804 needs a clock source to operate. The time taken to convert the analog value to digital value is dependent on this clock source. Always an external clock can be given at the Clock IN pin. ADC 0804 also has its own inbuilt clock which can be used in absence of external clock. A reliable RC circuit is connected between the Clock IN and Clock R pins to use the internal clock.

IV. Design of Control Module of FPGA

FPGA is the center of the whole system control, which controls the data acquisition system, storage. Therefore, according to the role of FPGA needs in the system, it realizes to control the data acquisition module, and UART interface module within the FPGA

A. ADC Communication

The communication between ADC0804 with other peripheral device is parallel bus communication. Parallel communication is a method of conveying multiple binary digits (bits) simultaneously. The Fig 2 illustrates the parallel communication between the transmitting and receiving side.

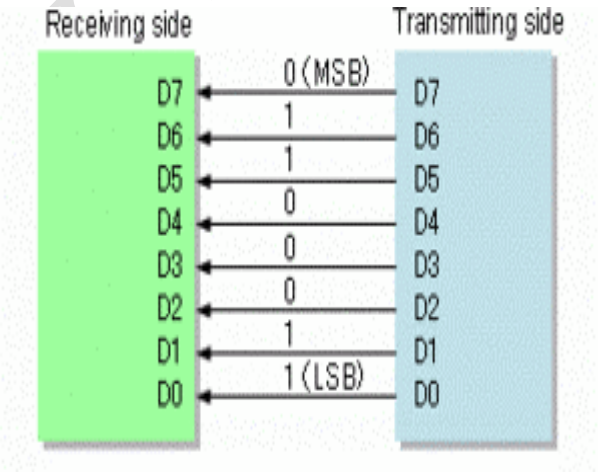

Fig -2: Parallel interface

B. ADC Communication with FPGA

The ADC communication with FPGA depends on three ADC signals namely, read, write and interrupt signals. The Figure 3 illustrates the connection between the ADC and FPGA.

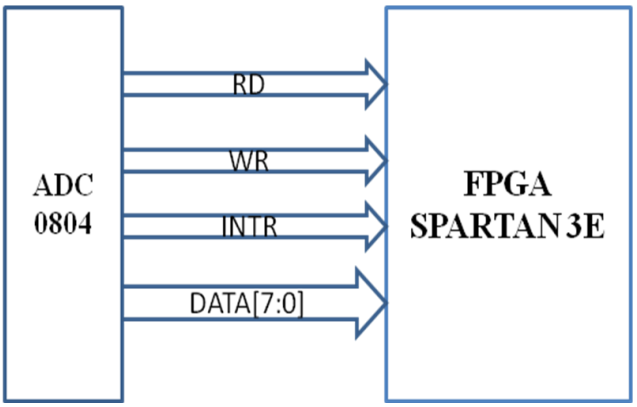

Fig -3: ADC and FPGA connection

C. Implementation of parallel bus

This protocol is the traditional type for most ADC. It has the advantage of the high speed throughput. This design uses ADC0804 for the peripheral device. Fig 4 illustrates the simulation of how the FPGA gets data from this ADC.
There are two main steps in the conversion process:

- The FPGA issues the start signal to activate the ADC then it will wait for the acknowledge signal.
- After finishing the data converting the ADC will send the acknowledge signal to the FPGA and FPGA reads the data from the bus. After that the FPGA gives the start signal to activate ADC again for getting the data on next read cycle.

Obviously, this data acquisition is so simple and fast. Thus, this protocol should be employed with the high speed system. Parallel bus protocol used in some particular applications where connections needs parallel line like Display/printer.
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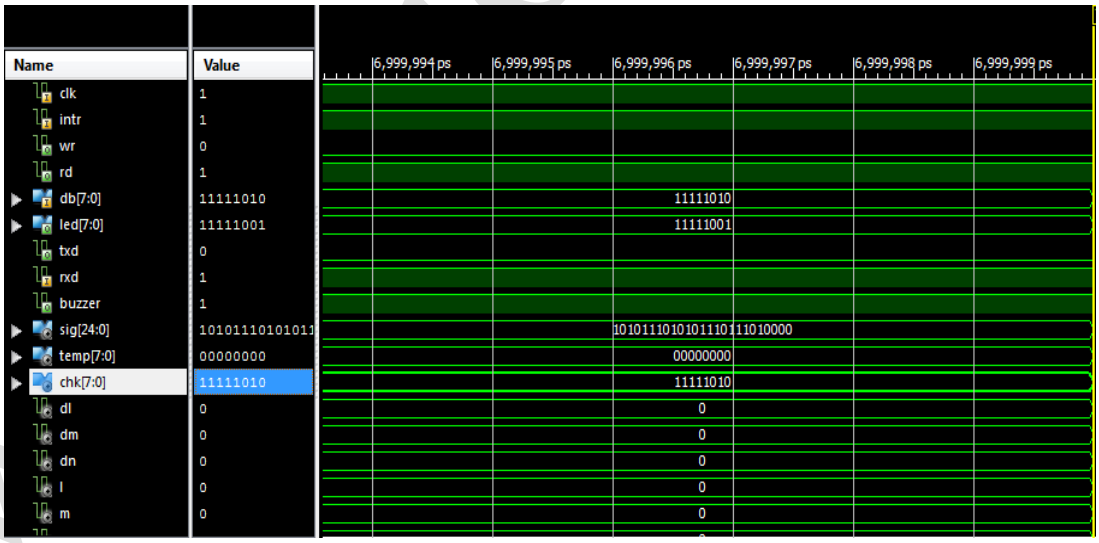

Fig -4: Simulation results of parallel ADC

Once FPGA starts getting all ADC data, then all the data's are transmitted to FPGA UART port for PC interface using RS 232. The Fig 5 illustrates the simulation results of UART

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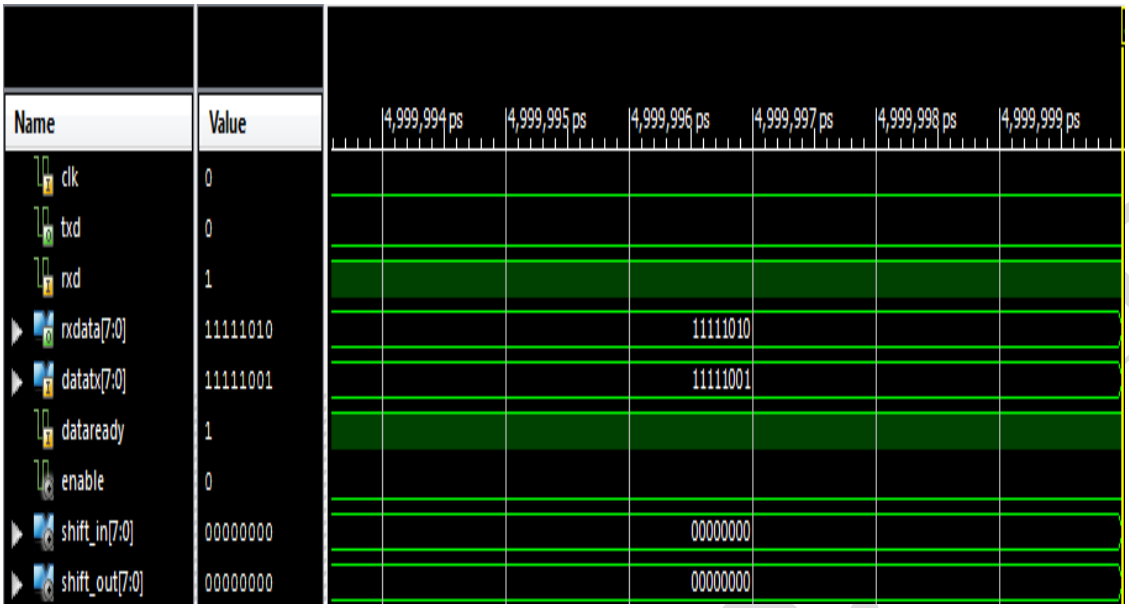

Fig -5: Simulation results of UART

V. PC INTERFACING

The FPGA is interface with PC using RS 232 serial communication. This RS 232 provides communication between the FPGA and PC. The application program allows user can interface with PC. The Fig 6 illustrates the communication between FPGA

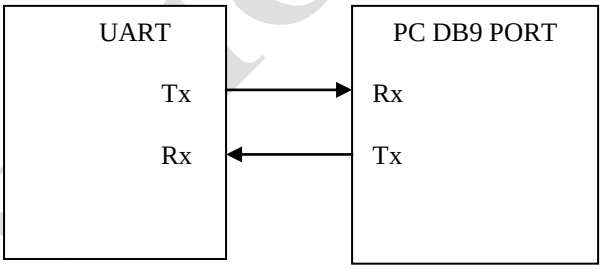

Fig -6:UART and PC connection

Hardware layer: Continuously sends the read request and it will return with one or more data, and put the data in a stack from which the data acquisition layer can read it.

Data acquisition layer: This used to collects the data, and save them into the PC. When this layer runs, it moves the data from the queue shared with the hardware layer into its own container, and updates the current value shared with the presentation layer.

This application is responsible to read data from ADC and presents them to the user in the style of both numeric value and also a graphic relationship. Fig 7 illustrates the operation of application program**.**

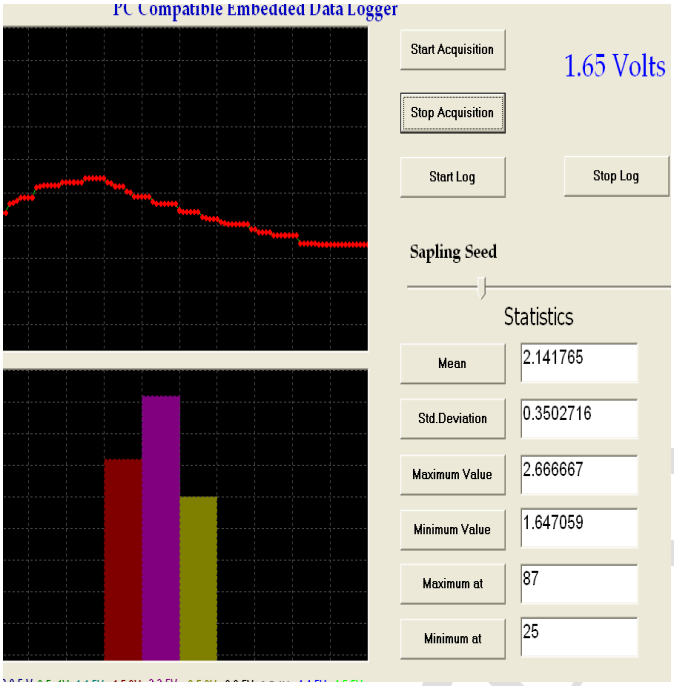

Fig -7: Operation of application program

VI. CONCLUSION

Using FPGA to control the entire work process and complete the data collection, processing, storage. We could claim that our data acquisition system is one of the useful solutions for the data acquisition. Having contained the input channels with a ADC protocols, our system can interface to the ADC input devices with any protocols to the PC independently. In addition, with an enormous number of the I/O ports in the FPGA, it is feasible to add more channels in the future.

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[6]

Authors Short Profile:

1. Thirunavukkarasu.T completed his Bachelor of Engineering at Jayam College Of Engineering and Technology, Dharmapuri, Tamil Nadu India in 2011.He is Pursuing Master in Engineering at Sri Ramakrishna Engineering College, Coimbatore, India.
2. Kirthika.N completed her M,E.at Anna university, Chennai, Tamil Nadu, India. She is working as Assistant Professor in the department of ECE (PG) at Sri Ramakrishna Engineering College, Coimbatore, India.