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CASCADED SWITCHED-DIODE TOPOLOGY USING TWENTY FIVE LEVEL SINGLE PHASE INVERTER WITH MINIMUM NUMBER OF POWER ELECTRONIC COMPONENTS

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***Abstract*— In this paper, cascaded switched-diode topology using twenty five level single phase inverter with minimum number of power electronic components are proposed, which can produce many level with minimum number of power electronics switches, gate drive circuits, power diodes, and dc voltage sources. The number of required power electronic switches against required voltage levels is a very important factor in designing of multilevel converter, because switches define the reliability, circuit size, cost, installation area, and control complexity. To produce maximum number of levels at the output voltage, the proposed cascade topology is optimized for different goals, such as the minimization of the number of power electronic switches, gate driver circuits, power diodes, dc voltage sources, and blocking voltage on switches. Comparison of the results of various multilevel converters will be investigated to reflect the merits of the presented topologies. The operations of the proposed multilevel converters have been analyzed with the experimental and simulation results for different topologies. Verification of the analytical results is done using MATLAB simulation.**

Keywords— ***Bi directional switch, cascade, full bridge converter, multilevel inverter, symmetric.***

I. INTRODUCTION

Multilevel power conversion was first presented over 30 years ago. Multilevel converters can produce a large number of output voltage levels, which results in high voltage capability, lower harmonic contents, lower switching losses, better electromagnetic compatibility, and high power quality. Multilevel converters have been used for several applications such as static reactive power compensation, adjustable speed drives, and renewable energy sources and so on .The principal function of multilevel converter is to synthesize a desired ac voltage from several separate dc sources. Many kinds of topologies for multilevel converters have been proposed. In general there are three types of multilevel inverter: 1) Neutral Point Clamped (NPC) converter.2) Flying Capacitor (FC) converter and3) Cascade H-bridge (CHB) converter.

The unequal voltage sharing among series connected capacitors is the main drawback of NPC converter. In addition, this structure needs a large number of clamping diode for higher levels. The FC converter requires a great number of storage capacitors for higher output voltage levels and the capacitors voltage balancing is difficult. Conventional cascade multilevel converter is one of the most important topologies in the family of conventional multilevel converters because cascade converter requires the least number of components, when compared with the flying capacitor and diode clamped converter. A cascade multilevel converter consists of the number of H-bridge converter units with separate dc sources for each unit, which connected in cascade or series.
In symmetric cascaded multilevel converter, dc voltage sources values of similar cells are equal. For the same number of power devices, asymmetric cascade multilevel topology significantly increases the number of output voltage levels. In these topologies, the values of dc voltage sources of different cells are non-equal however; the symmetric and asymmetric CHB converter requires a large number of switches and dc voltage sources.

An attempt has been made into propose a new structure for multilevel converter with reduced number of power electronic components comparison with conventional cascade converter. This converter needs a large number of bidirectional switches. In addition, the magnitude of blocked voltage by bidirectional switches is high.

In another new topology for cascade multilevel converter has been introduced, which reduces the number of bidirectional switches, power diodes, and dc voltage source in comparison with proposed topology. This topology consists of several sub

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multilevel converters and full-bridge converters. But, this topology requires a large number of bidirectional switches and gate driver circuits.

In this paper, new topologies for symmetric, asymmetric and cascade switched-diode multilevel inverter are proposed, which have more advantages in comparison with presented topologies.

II. System Structure and Analysis

A. BLOCK DIAGRAM

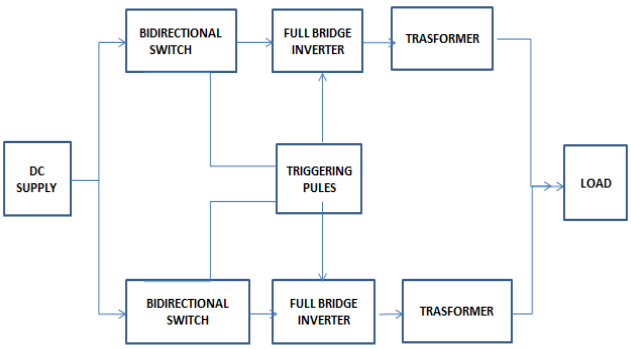

Fig.1. Block diagram for CMI

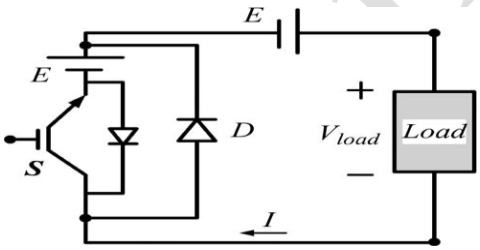

Fig.2.Basic circuit of proposed switched-diode multilevel converter.

III. Basic of Proposed Multilevel Converter Topologies

Fig. 2 shows the basic topology for proposed switched-diode multilevel converter. In this circuit, when the switch S is turned off, the current flows from the diode *D* and load voltage will be *E*. But, when the switch *S* is turned on, the diode is reverse biased and current flows from the voltage source *E* and loadvoltage will be (2*E*). By the use of this method, the loadvoltage is controlled. This method is the basic of proposed multilevel converter. The new presented structures in threedifferent topologies are introduced and consist of: 1) Symmetricswitched-diode multilevel converter; 2) Cascade switched diode multilevel inverter.

IV. Symmetrical Switched-Diode Multilevel Inverter

The structure of proposed symmetric switched-diode multilevel inverter is shown in Fig.3. In this structure, the values of the dc voltage sources are equal. Therefore, this topology is called symmetric switched diode multilevel converter. Table I gives the values of output voltages (Eo) for different states of switches.

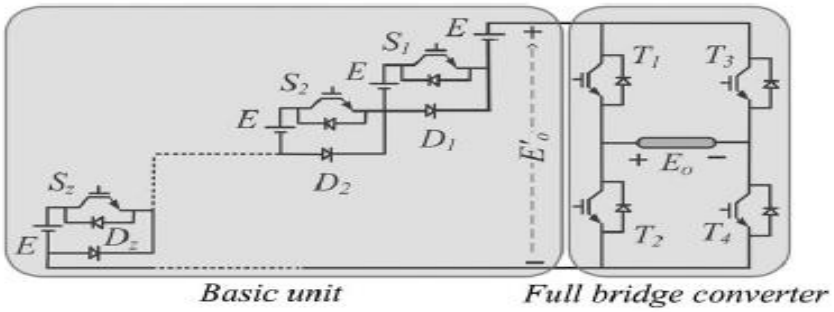

Fig.3. Asymmetrical switched-diode multilevel converter topology

Table I Switch State for Symmetric Topology

State	Switches states									Output voltage
	S_1	S_2	.....	S_{z-1}	S_z	T_1	T_2	T_3	T_4	
1	0	0	.....	0	0	1	0	1	0	0
2	0	0	.....	0	0	1	0	0	1	E
3	0	0	.....	0	0	0	1	1	0	$-E$
4	1	0	.....	0	0	1	0	0	1	$2E$
5	1	0	.....	0	0	0	1	1	0	$-2E$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2K$	1	1	.....	1	1	1	0	0	1	KE
$2K+1$	1	1	.....	1	1	0	1	1	0	$-KE$

In this topology, the basic unit generates a staircase voltage waveform (Eo) withpositive polarity (E, 2E, 3E, ...). It is connected to a full bridge converter, which particularly alternates the input voltage polarity and generates positive or negative staircase waveform (Eo) at the output voltage (0, E,2E,3E, ...).The number of output levels (***N****level)*, IGBTs (***N****IGBT)*, and the maximum output voltage (Eo,max) in the proposed symmetric converter are obtained as follows, respectively:

N_{level}=2K + 1 (1)
N_{IGBT} =K + 3 (2)
$E_{o,max}$=KE. (3)

Where K represents the number of dc voltage sources. Compare the number of IGBTs versus the number of output levels (***N****level*) in the proposed symmetric switched-diode topology and the symmetric conventional cascade topology. This figure shows that the proposed converter requires the least number of IGBTs.

V. ASYMMETRICAL SWITCHED-DIODE MULTILEVEL CONVERTER

Asymmetrical multilevel converter provides an increased number of output voltage levels for the same number of power electronic devices than its symmetric counterpart. In for dc voltage sources of conventional cascade H-bridge topology, two main methods have been suggested, which have been called binary and trinary configuration. The trinary configuration can produce a great number of levels in comparison with binary configuration. Fig. 4 shows the proposed topology for asymmetrical switched-diode converter, which consists of one basic unit and a full-bridge converter.

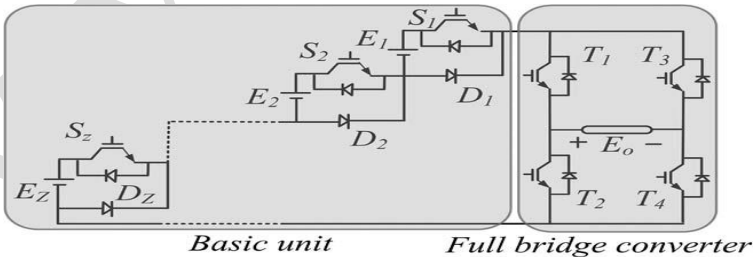

Fig. 4.Proposed asymmetrical switched-diode multilevel converter topology.

Table II shows the ON switches look-up table for proposed asymmetric topology.
In this topology, the values of dc sources are suggested to be chosen according to the following algorithm:

$$E1 = E \quad (4)$$
$$Ej = 2(j-1)E \text{ For } j = 2, 3, 4, \ldots, Z. \quad (5)$$

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TABLE II SWITCH STATES FOR ASYMMETRICAL TOPOLOGY

state	Switches states									Output voltage
	S_1	S_2	----	S_{z-1}	S_z	T_1	T_2	T_3	T_4	
1	0	0	----	0	0	1	0	1	0	0
2	1	0	----	0	0	1	0	0	1	E_1
3	1	0	----	0	0	0	1	1	0	$-E_1$
4	0	1	----	0	0	1	0	0	1	E_2
5	0	1	----	0	0	0	1	1	0	$-E_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2Z	0	0	----	1	1	1	0	0	1	E_z
2Z+1	0	0	----	1	1	0	1	1	0	$-E_z$
2Z+2	1	1	-----	0	0	1	0	0	1	(E_1+E_2)
2Z+3	1	1	----	0	0	0	1	1	0	$-(E_1+E_2)$
⋮	⋮	⋮	----	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2^{(Z+1)}-2$	1	1	----	1	1	1	0	0	1	$(E_1+E_2+\ldots+E_z)$
$2^{(Z+1)}-1$	1	1	----	1	1	0	1	1	0	$-(E_1+E_2+\ldots+E_z)$

For this method, the number of levels and maximum output voltage are given by (6) and (7), respectively

$$Nlevel=2(Z+1)-1 \quad (6)$$
$$Eo,\max=(2Z-1)E \quad (7)$$

Where Z represents the number of dc sources. In the proposed asymmetric topology, the number of IGBTs is obtained by

$$N_{IGBT}=Z+4. \quad (8)$$

Fig. 5 shows the comparison between proposed asymmetric switched-diode topology with trinary configuration of conventional cascade. This comparison shows that the proposed asymmetric switched-diode converter generates the maximum number of level with fewer numbers of switches. It is important to note that the proposed symmetric and asymmetric switched-diode topologies can be used in renewable energy sources and medium-voltage applications. However, this structures needs several dc voltage sources. For renewable energy source applications, instead of dc voltage sources, we can use photovoltaic panels. In this application, capacitor voltage balancing is important. For example, in fuel cells, the output voltages are changed during the converter performance and lead to reduction of the quality of output voltage in dc-link of converter. This circuit consists of an ac voltage source, multistep transformer, and several rectifiers. The proposed symmetric and asymmetric switched-diode topologies use only one full-bridge converter, which is a restriction for high-voltage applications. In addition, these topologies need more number of devices.

VI. ASCEDE SWITCHED-DIODE MULTILEVEL INVERTER

To provide a large number of levels with less number of components, cascade switched-diode multilevel converters can be used.

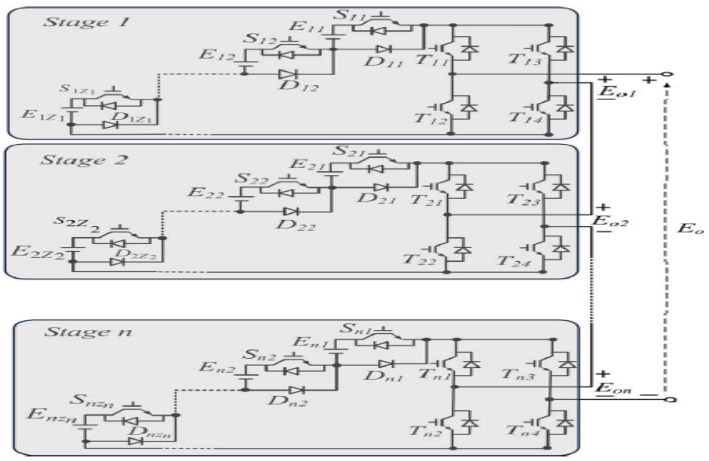

Fig.5. Cascade switched-diode multilevel converter topology.

Fig.5. shows the structure of proposed cascade multilevel inverter. The output voltage of the proposed cascade switched diode multilevel inverter is given by

Eout=Eo1+Eo2+・・・+Eon.(9)

For the proposed cascade topology, two methods for determination of values of the dc sources are presented.

VII. Twenty-Five Level Cascade Switched- Dioide Multilevel Inverter

Fig. shows a Twenty five-level cascade converter topology structure based on the first method of proposed cascade topology (see Fig 3.). It is noticeable that if the values of dc sources in this topology are determined using the method of proposed topology (see Table 1),

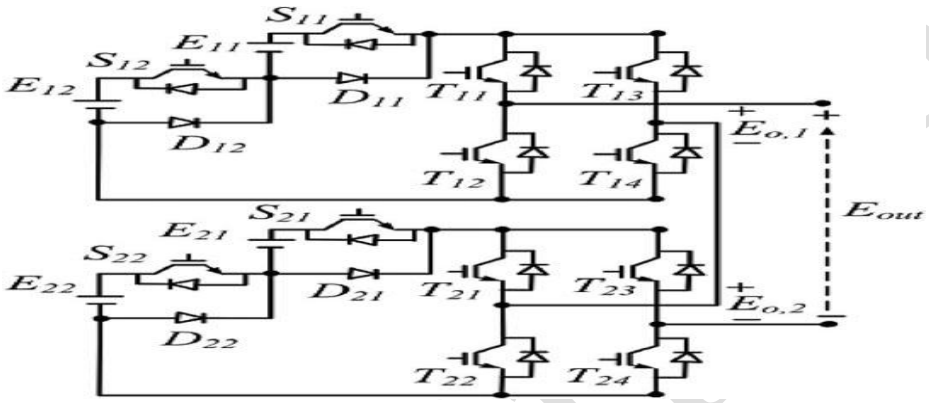

Fig.6. Twenty-five-level cascade converter.

The comparison of THDs of output voltage and current in the two topologies shows that increasing the number of levels leads to the multilevel converter producing output voltage waveform with very low THD.

VIII. Simulation Results

This section deals with the simulation results for symmetric and cascaded switched-diode multilevel inverter topologies. First, the simulation results for a symmetric switched-diode inverter are presented. Then, the simulation results for a 25-level cascade switched-diode inverter are presented. For all of the studies, test has been made on the R- load .The value of output voltage frequency is 50 Hz.

A. TWENTY FIVE LEVEL CASCADE MULTILEVEL INVERTER CIRCUIT

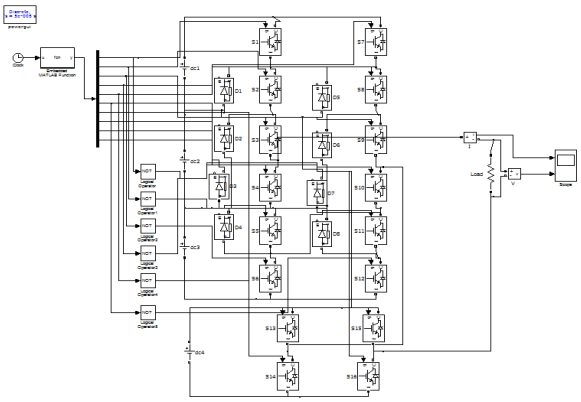

Fig.9. Simulation of Twenty Five- Level Cascade Multilevel Inverter

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OUTPUT VOLTAGE AND CURRENT WAVE FORM TWENTY FIVE LEVEL CASCADE MULTILEVEL INVERTER CIRCUIT

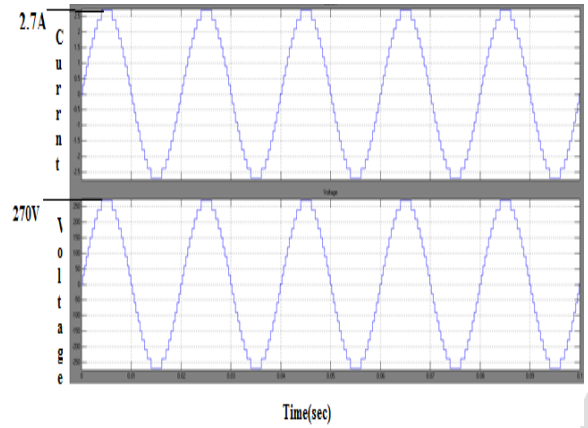

Fig .10 **(a)**

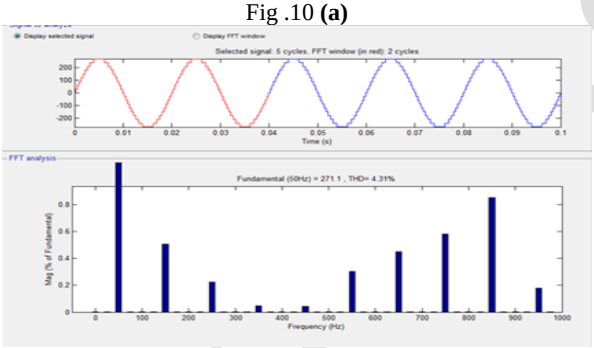

Fig.10 (b)

Fig.10. Simulation waveform of 25-level cascade multilevel inverter (a)Output voltage and current waveform (b) Output voltage and harmonic spectrum (THD = 4.50%).

B. MODIFIED TWENTY FIVE-LEVEL CASCADE MULTILEVEL INVERTER WORK

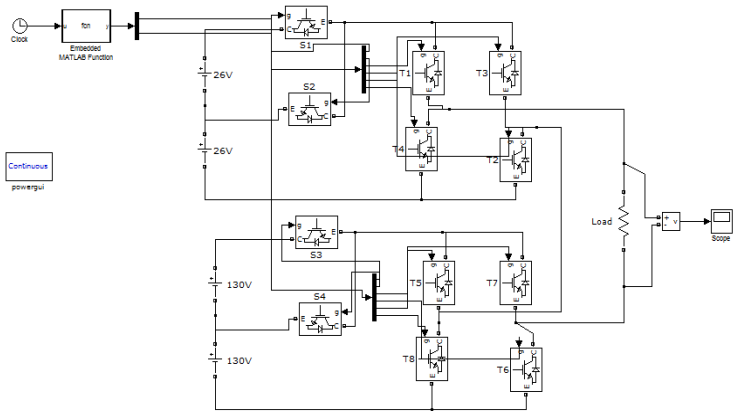

Fig.11. Simulation for Modified Twenty Five- Level Cascade Multilevel Inverter

OUTPUT VOLTAGE AND CURRENT WAVEFORM FOR MODIFIED TWENTY FIVE-LEVEL CASCADE MULTILEVEL INVERTER WORK

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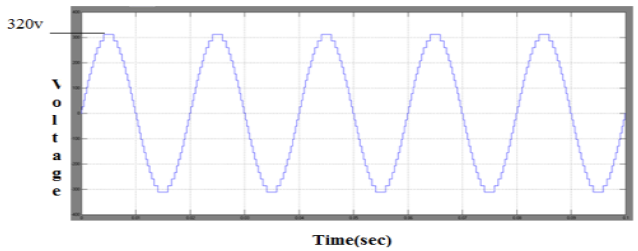

Fig.11. (a)

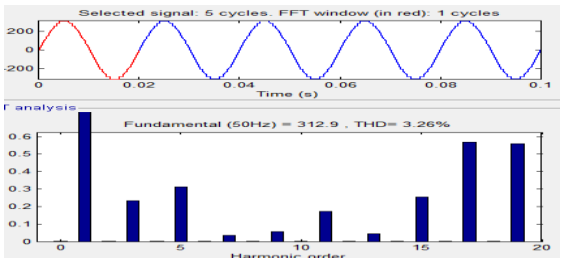

Fig.11. (b)

Fig.11.Simulation waveform of modified 25-level cascade multilevel inverter (a)Output voltage and current waveform (b) Output voltage and harmonic spectrum (THD = 3.26%).

C. SIMULATION FOR CASCADE MULTILEVEL INVERTER CONNECTED TO MOTOR

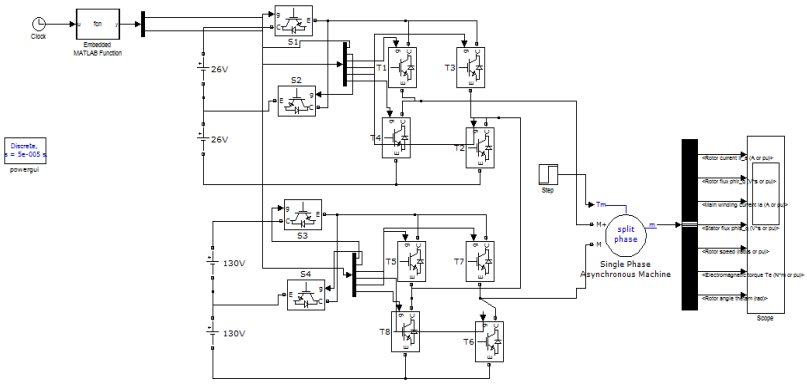

Fig.12. Simulations for Cascade Multilevel Inverter Connected To Motor
OUTPUT FOR CASCADE MULTILEVEL INVERTER CONNECTED TO MOTOR

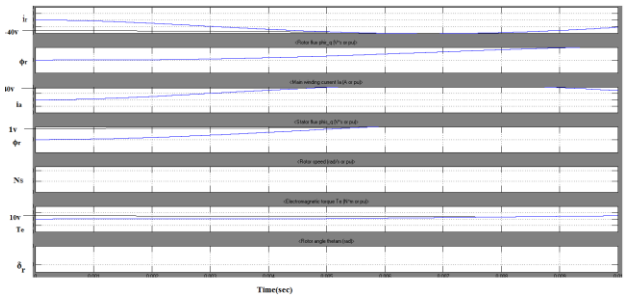

Fig.12. (a)

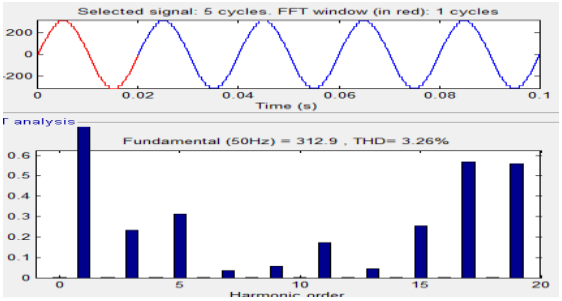

Fig.12. (b)

Fig.12.Simulation result for cascaded multilevel inverter connected to motor in rotor current, rotor voltage, main winding current, stator flux, rotor speed, electromagnetic (THD = 3.26%).

IX. Comparision of Results

PARAMETER	25 -LEVEL CMI	MODIFIED 25-LEVEL CMI	MODIFIED 25-LEVEL CMI CONNECTED TO MOTOR
INPUT VOLTAGE	270V	312V	312V
THD VAULE	4.31%	3.26%	3.26%
COMPONENT	Large Number of power electronic switches, gate driver circuits, power diodes,	Minimum Of power electronic switches, gate driver circuits, power diodes, and dc voltage sources.	Minimum of power electronic switches, gate driver circuits, power diodes, and dc voltage sources.

X. Conclusion

This paper proposes new topologies for symmetric, asymmetric, and cascade switched-diode twenty five level converter with reduced number of components. The proposed cascade structure extends the design flexibility and the possibilities to optimize the converter for different objectives such as the minimization of the number of IGBTs, gate driver circuits, dc voltage sources, standing voltage on switches, and power diodes. Less number of the switches leads to the reduction of size, simple control strategy, and high efficiency. Comparison among the proposed converters with conventional cascade and other similar topologies was provided. It was shown that the proposed topologies can produce many levels with fewer components.

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