

AN EFFICIENT VLSI ARCHITECTURE BASED AUTOMATIC VENDING MACHINE USING FPGA

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Abstract— Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. The digital architecture is mainly used in all type of real world application architectures and thus the architecture to modified based on the enhancement purpose. Finite State Machine (FSM) modeling is the most crucial part in developing proposed model as this reduces the hardware. Vending machines are used to dispense small different products, when a coin is inserted. These machines can be implemented in different ways by using microcontroller and FPGA board. Here in this paper, we proposed an efficient algorithm for implementation of vending machine on FPGA board. Because FPGA based vending machine give fast response and uses less power than the microcontroller based vending machine. The FPGA based vending machine supports four products and three coins. The vending machine accepts coins as inputs in any sequence and delivers products when required amount is deposited and gives back the change if entered amount is greater than the price of product. This technique has been tested using Xilinx v 14.2 software packages using Very High Speed Integrated circuit hardware description language (VHDL), RTL and technology schematic are included to validate simulation results.

Keywords— FSM, VHDL, Vending Machine

I. INTRODUCTION

A vending machine is a machine that provides items such as four different products even Diamonds and platinum jewelry to customers, after the vendee inserts currency or credit into the machine using extremely simple steps. These steps would not be time consuming at all. The vendee would get all the details on the screen which he/she should follow. Previous microcontroller or Microprocessor based vending machines were inefficient as compared to FPGA based vending machine. So it is necessary to make it more reliable with efficient algorithm that will be fully commanded by FPGA based solution. The main purpose of this project was to create a vending machine which could provide four different snacks products to the people using extremely simple steps. We have made an attempt to vend four products of different prices in the same machine.

The machine will also provide the change to the vendee depending on the amount of money he/she has inserted. It is also possible to withdraw the deposited money in between, if consumer wishes by pressing a cancel button. VHDL is a versatile and powerful hardware description language which is useful for modeling electronic systems at various levels of design abstraction and in electronic design. Automation to describe digital and mixed signals systems such as FPGA and Integrated Circuits. The abbreviation of VHDL is VHSIC (Very high Speed Integrated Circuit) Hardware Description Language, it is an industry standard language used to describe hardware from the abstract to the concrete level. In the proposed vending machine Bottom up methodology of VHDL is used. A FPGA is a semiconductor device that is made up of reprogrammable logic components. These logic components are made up of a combination of look-up tables (LUT) and flip-flops (FF). The role of the sensors is to measure physical properties of the coins, such as dimensions, conductivity, magnetic permeability, elasticity, etc., and even the existence or not of relief. Only the diameter of the coin, actually its secant, can be directly measured, while for the remaining parameters only indirect information is obtained. The sensors are located along this path, and their signals have to be processed to decide if the coin is good or a fake before it reaches the end of the ramp, where the coin is driven to the storage or returned to the customer.

II. RELATED WORK

The current state of the machine is stored in the state memory, a set of n flip-flops clocked by a single clock signal (hence “synchronous” state machine). The state vector (also current state, or just state) is the value currently stored by the state memory. The next state of the machine is a function of the state vector and the inputs. Mealy outputs are a function of the state vector and the inputs while Moore outputs are a function of the state vector only. Design Compiler directly supports finite-state machines using the extract command.

Extract gives you the ability to change your state encodings during compile, thus allowing you to experiment with different FSM implementations.

The vending machines are more accessible and practical than the conventional purchasing method. Nowadays, these can be found everywhere like at railway stations selling train tickets, in schools and offices vending drinks and snacks. The FPGA based vending machine is also programmable and can be reprogrammed whereas in the Embedded based machines we have to change the whole architecture of the machine if we want to change or enhance the design of the machine. This machine also has a “Cancel Request” feature which provides the user to withdraw/cancel the request and return back the money to the user. The user will get a bill of total number of products.

III. DESIGN METHOD

A. Conventional Design

The state diagram consists of four states (user selection, waiting for the money insertion, product delivery and servicing, (when product not available = '1')). Initially, when the reset button is pressed, the machine will be ready for the user to select the product. After this the user selects the product which is to be dispensed. This state can be one of the sel_1, sel_2, sel_3 and sel_4. Firstly, the machine will check the availability of the product. After this, the control unit will move to the waiting state, where it will wait for the insertion of money.

The machine can accept only two types of notes i.e. rupees 10/- and 20/-. Let us suppose that the user selects sel_1 input. The machine will firstly check that whether the products are available in the machine or not. After this the control unit will move to the waiting state, where it will wait for the money to be inserted.

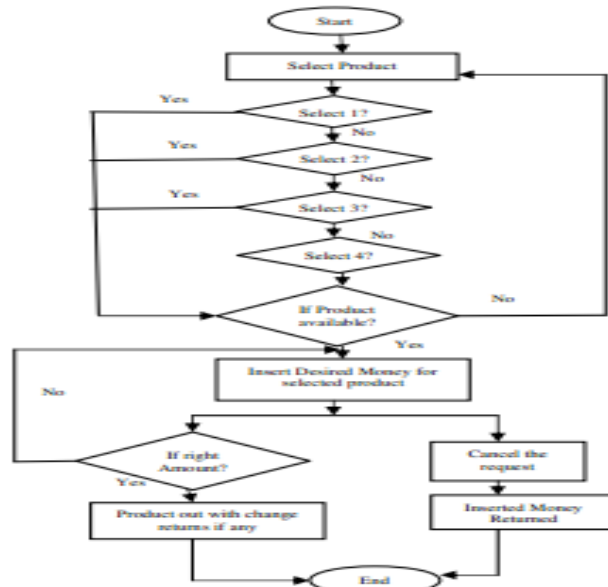


Fig1. Flow chat for vending machine

Then if rupees 10/- note is inserted then the machine will go to state_1 and wait until the desired money is inserted. And if rupees 20/- note is inserted the machine will move to state_2 and then wait until 30/- rupees are inserted to the machine. There

is a feature added to it, which withdraw request if the user does not want to take the product, and when the cancel button is pressed by the user the inserted money will be return back to the user through the return output.

B. System Design

In this system design using set of modules will be followed in the architecture. These modules are clock and reset control, counter process, FSM Function, selection process, output process.

System architecture is shown in figure 2

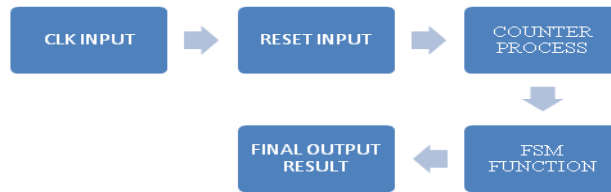


Fig 2. System Architecture

FSM Function

The finite state machine condition is used to change the state position in system architecture. This architecture mainly focused by the state position. The FSM position based on the present state and the previous state position level. And to optimize the state processing condition level. The FSM condition is to change the every timing for required state machine position level.

A set of States – the FSM is in one state at any time Inputs – inputs used by the FSM Next state function – Determines how the FSM moves from one state to another based on the state and the inputs. Output function – Compute the output based on current state (and possibly the inputs).The FSM transitions from one state to another as determined by the next state function function.

Selection Process

There is also an additional feature of withdrawing the request if the user doesn't want to take the product. When cancel button is pressed then the money inserted will be returned to the user through the return output. A money count signal is used for calculating the total money inserted in the machine. And if the money inserted is more than the money of the product then the extra change will be returned to the user.

C. Proposed Design

FSM for the best operating of the vending machine. So this structure has about 36 states which have been implemented using VHDL language and for Verilog HDL we have about 26 states.

In this design we are initializing with logic with money inserted concept i.e. if only if least money (money=5) has been inserted then only the items will be displayed directly for the selection process.

In FSM or finite state machine the output of the circuit is defined as a different set of state. In FSM the state register holds the state of machine and a next state logic which decodes the next state. The output register of FSM defines machine's output.

In FSM based machines the algorithm can be explained in one process because the hardware get reduce. Money signal is also seven bits wide. At every transition, money count which is an internal signal can be updated and this signal is also seven bits wide. The change will be returned through the change output signal when the inserted money is more than the total money of product clk and reset are also two input signals.

IV. SIMULATION RESULTS

Simulation result of automatic vending machine output shows in fig3.

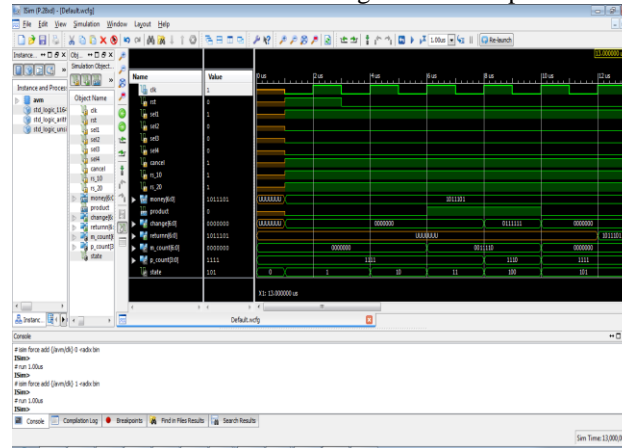


Fig 3.Simulation result of AVM output

Fig 4 and 5 shows that RTL and Technology schematic diagram

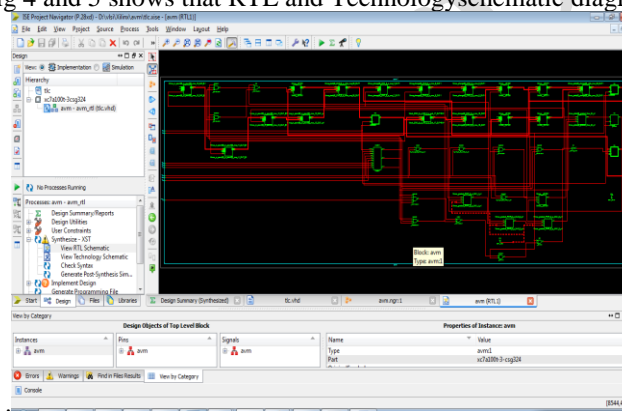


Fig4.RTL Schematic Diagram

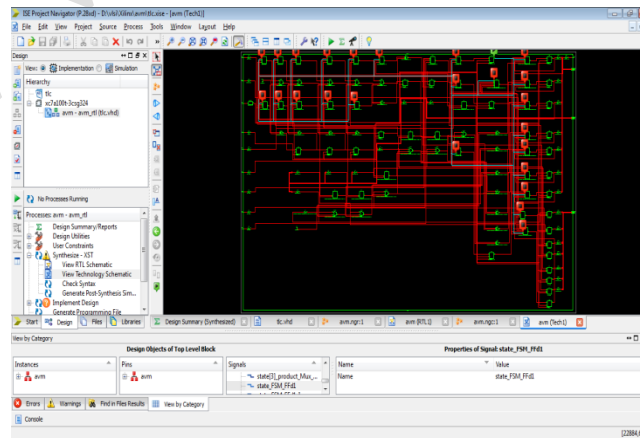


Fig 5. Technology Diagram

V. CONCLUSION

The presented FPGA based proposed vending machine is implemented using bottom-up approach methodology. The design is verified on the FPGA Spartan 3 development Board. Vending Systems enhances productivity, reduces system development cost, and accelerates time to market also FPGA based vending machine give fast response and easy to use by an ordinary person. The designed machine can be used for many applications.. Finite State Machine (FSM) modeling is the most crucial part in developing proposed model as this reduces the hardware.

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