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An Improved Multiple Single Input Change Sequence Generator

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Abstract*— When the circuit size progresses with increase in technology, the testing time of the circuit also increases. So Automatic Test Equipment (ATE) was proposed to meet the insatiable demand of cost and further In-Situ testing scheme such as Built In Self Test(BIST) was proposed later to further optimize the cost. This paper proposes an Improved Multiple Single Input Change sequence generator (IMSIC) which is a part of BIST. The proposed test pattern generator generates test sequences by performing EXOR operation between the Johnson counter and the traditional LFSR. Moreover, Vector re-ordering algorithm has been incorporated in order to meet the fault coverage with minimum test length duration and the included genetic algorithm also found the best seed to give the targeted fault coverage with less time duration for testing. As a result, low power testing and the same with less testing duration has been achieved in this paper. The results were validated using UMC 90 nm Technology library.

Keywords*— DFT-BIST-LFSR-CUT-ATPG-SIC-BILBO.

I. INTRODUCTION

The increasing demands for high-density and high performance integrated circuits dictate the Built-In Self Test (BIST) schemes to guarantee high fault coverage, which is expected to be produced by a simple test-pattern generator in an acceptable number of vectors. The BIST involves performing the test-vector generation and the output-response analysis on a chip through the built-in hardware. BIST is a powerful Design For-Testability (DFT) technique for addressing highly complex Very-Large-Scale Integration (VLSI) testing problems. BIST designs include on-chip circuitry to provide test patterns and analyze output responses. Performing tests on the chip greatly reduces the need for complex external equipment. The main motivation for considering power consumption during testing is generally, a circuit consumes much more power in test mode than in normal mode. BIST techniques are mainly employed to improve the circuit's fault coverage, test application time, and test development efforts. In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems.

However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation.

II. ENERGY AND POWER MODELING

Power consumption in CMOS circuits can be static or dynamic. Leakage current or other current drawn continuously from the power supply causes static power dissipation. Dynamic dissipation occurs during output switching because of short-circuit current, and charging and discharging of load capacitance. For existing CMOS technology, dynamic power is the dominant source of power consumption, although this might change for future high-scale integration. The average energy consumed at node *i* per switching is $½C_iV^2_{DD}$, where C_i is the equivalent output capacitance, and VDD is the power supply voltage. Therefore, a good approximation of the energy consumed in a period is $½C_{isi}V^2_{DD}$ where *si* is the number of switching during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, as a first approximation we assume capacitance *Ci* to be proportional to the fan-out of node . Therefore, an estimation of the energy *Ei* consumed at node *i* during one clock period is $Ei = 1/2FiCoV^2_{DD}$, where C_o is the circuit's minimum parasitic capacitance. According to this expression, estimating energy consumption at the logic level requires the calculation of fan-out *Fi*.[8]

III. TERMINOLOGY

Test power is a possible major engineering problem in the future of System on Chip (SoC) development. As both the SoC designs and the deep-submicron geometry become prevalent, larger designs, tighter timing constraints, Higher operating frequencies, and lower applied voltages all affect the power consumption systems of silicon devices. [9]

A. Energy

The total switching activity generated during test application, energy affects the battery lifetime during power up or periodic self-test of battery-operated devices.

B. Average power

Average power is the total distribution of power over a time period. The ratio of energy to test time gives the average power. Elevated average power increases the thermal load that must be vented away from the device under test to prevent structural damage (hot spots) to the silicon, bonding wires, or package.

C. Instantaneous power

Instantaneous power is the value of power consumed at any given instant. Usually, it is defined as the power consumed right after the application of a synchronizing clock signal.
Elevated instantaneous power might overload the power distribution systems of the silicon or package, causing brown-out.

D. Peak power:

The highest power value at any given instant, peak power determines the component's thermal and electrical limits and system packaging requirements. If peak power exceeds a certain limit, designers can no longer guarantee that the entire circuit will function correctly. In fact, the time window for defining peak power is related to the chip's thermal capacity, and forcing this window to one clock period is sometimes just a simplifying assumption. For example, consider a circuit that has peak power consumption during only one cycle but consumes power within the chip's thermal capacity for all other cycles. In this case, the circuit is not damaged, because the energy consumed which corresponds to the peak power consumption times one cycle will not be enough to elevate the temperature over the chip's thermal capacity limit (unless the peak power consumption is far higher than normal).

IV. EXISTING METHODS

Weighted pattern generation inserts a combinational circuit between the output of the Pseudo-Random Pattern Generator (PRPG) and the Circuit Under Test (CUT) to increase the frequency of occurrence of one logic value while decreasing the other logic value. This approach may increase the probability of detecting those faults that are difficult to detect using the typical LFSR pattern generation technique. Although weighted pattern generation is simple in design, achieving adequate fault coverage for a BIST circuit remains a problem.[10]

When BIST is performed during manufacturing test where a tester is present. Hybrid BIST involves combining BIST and external testing by supplementing the pseudo-random patterns with deterministic data from the tester to improve the fault coverage. The simplest approach is to perform top-up ATPG for the faults not detected by BIST. To obtain a set of deterministic test patterns that "top-up" the fault coverage to the desired level and then store those patterns directly on the tester. In a system-on-chip, test scheduling can be done to overlap the BIST run time with the transfer time for loading the deterministic patterns from the tester. Hybrid BIST schemes have been developed, which attempt to store the deterministic patterns on the tester in a compressed form and then make use of the existing BIST hardware to decompress them. The test vectors reordering techniques aim to reduce the switching activity by modifying the order of the scan chain, in which the number of transitions between two consecutive vectors is reduced (i.e. the Hamming distance between two consecutive vectors is minimum), then the weighted switching activity(WSA) will be reduced in the whole CUT. The technique aims to reorder the test vectors in such a way to reduce the number of transitions between the consecutive vectors before applying them to the CUT's primary inputs.[1]

Test cubes are test vectors where the values of some bits are left unspecified as X's (don't care bits) for example 1X00X1 is a test cube. In scan-based BIST, a test vector that detects many targeted faults may contain many don't care bits (X). In conventional scan ATPG each X bit is filled with a 0 or 1 randomly since this will not affect the fault coverage. In fact the number of X bits in each test cube is typically high . The main aim of such techniques is to assign a value to the X bits in the test cube so that the number of the transitions in the scan cells is minimized, hence reducing the transitions in the scan-cells, which leads to a reduction in the overall switching activity in the CUT during shift cycles .[2],[3]

V. PROPOSED METHOD

The overall block diagram includes Multiple Single Input Change sequence (MSIC) generator and vector reordering module. As soon as the test pattern generator generates the test sequences, the test patterns are reordered before it is applied to the circuit under test. Here, the seed sequence generator generates the test patterns by loading its seed value when the reset signal is given. Test patterns which are coming from seed sequence generator are simultaneously added with the Characteristic Sequence Generator. The addition operation refers to modulo-2 addition. Further, the located Gray counter inside the characteristic sequence generator generates patterns by the logic block which is controlled by the clock signal. The placed vector reordering module helps in reducing the unwanted transitions during testing. As a result, average power consumption of the circuit during testing was reduced.

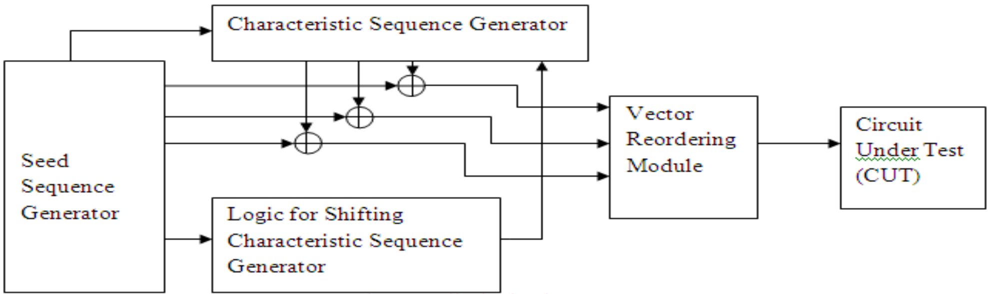


Fig Overall Block Diagram

A. Seed sequence generator

The seed sequence generator is nothing but a simple Linear Feedback Shift Register (LFSR). The model of LFSR considered here is of external type in which the co efficient are represented by c which ranges from 1 to n. In general any LFSR can be represented by a polynomial equation which is represented as follows [4]

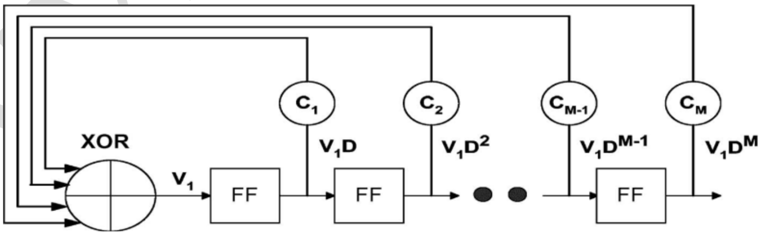


Fig. 2 LFSR

$V_1 = C_1 V_1 D^1 \oplus C_2 V_1 D^2 \oplus \cdot\cdot\cdot \oplus C_M V_1 D$.....(1)

where, $V_1 D^i$, i = 1, . . . , M is the ith delay of flip flop.

Ci, i = 1, . . . , M represents whether the $V_1 D^i$ is connected to the XOR gate or not.

Here while Implementing Built in Self Test (BIST) for C17 bench mark circuit, the LFSR considered is four bit and loads initial sequence as 1010 pattern. The corresponding polynomial equation is represented as

$V_1 = 1 \oplus C_1 V_1 D^1 \oplus C_2 V_1 D^3$ .....(2)

B. Characteristic Sequence Generator

The characteristic sequence generator is a binary to gray counter. The counter receives input from binary counter and the logic module establishes synchronization with the seed sequence generator.[5],[10]

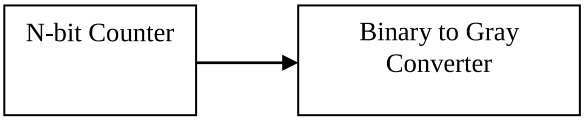


Fig. 3 Characteristic sequence generator

C. Vector Reordering Module

The vector re-ordering module contains hamming distance calculator and logic for arranging the test patterns with minimum hamming distance. In case of a Test Per Clock architecture the logic inside the module further prevents the transition that will happen inside the CUT by performing filtering operation until SIC sequence is achieved. Therefore power consumption along with the testing time gets optimized. Further optimization is also possible by incorporating reseeding capability to the LFSR because of that the fault present in the circuit is detected with lesser time duration than actually needed.

D. BIST (BILBO) Architecture

Most of the logic BIST schemes are based on the STUMPS (Self-Test Using a MISR and Parallel Shift register) structure, which applies random patterns generated by a hardware pattern generator to a full-scan circuit in parallel and compresses the responses in to a signature with a MISR. The basic BIST flow includes initialization and a shift capture loop.[6][7]

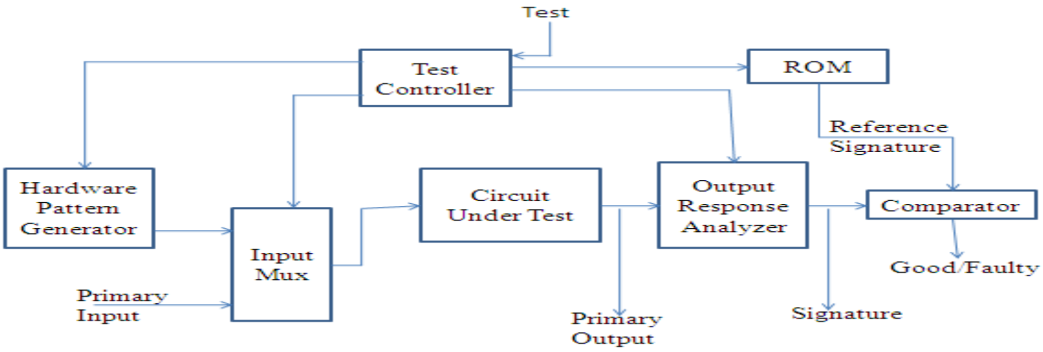


Fig.4 BIST Block Diagram

Figure 4 shows The basic blocks that form the BIST are LFSR (Linear Feedback Shift Register), DUT (Device Under Test), MISR (Multiple Input Signature Register), BIST controller and signature analyzer.

E. BIST Controller

BIST controller coordinates the operations of different blocks of the BIST. Based on the test mode input to the controller, the system either operates in the normal mode or in the test mode. When the test mode is enabled, the system enters the test mode, it gives enable signal to the LFSR which generates the patterns and then it gives enable signal to MISR for the compression of patterns from the DUT.

VI. RESULTS AND DISCUSSION

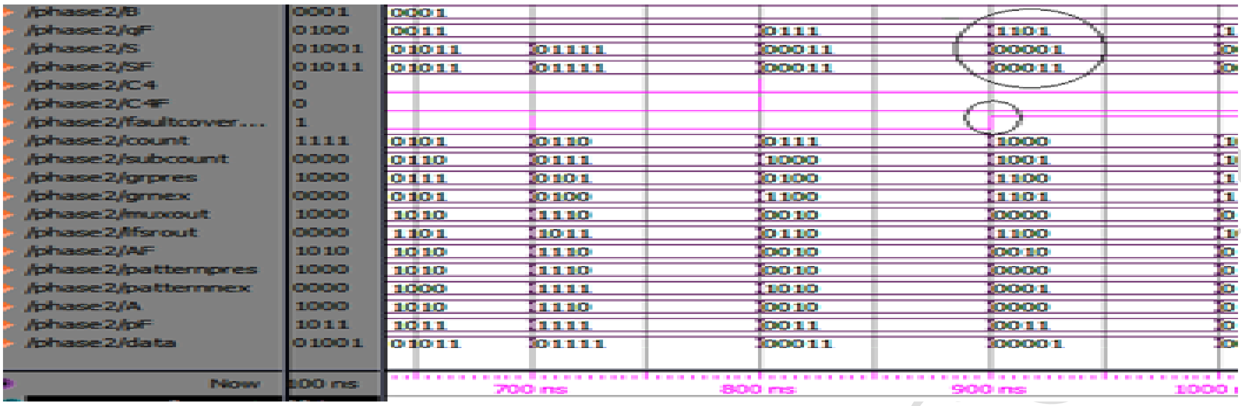


Fig. 5 Simulation result of BIST

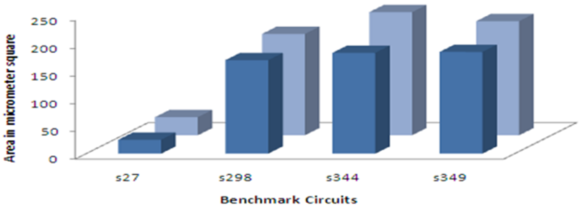
The Figure 5 Shows the simulation result for BIST architecture. Here the architecture incorporates TI7483 Benchmark circuit, for that the input A1 bit is Stuck At with 1 and the input b is fixed as 0001.The encircled portion denotes that detected fault for difference in sum value output.

A. DFT Compiler output

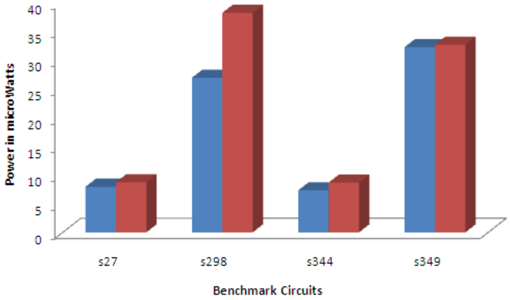
Circuit Name	Design compiler output(area in micrometer square)	Design compiler output(power in micro Watts)	DFT compiler output(area in micrometer square)	DFT compiler output(power in micro Watts)
s27	25.06415	7.9463	32.7265	8.7265
s298	168.660944	26.903	183.000	38.2079
s344	182.4516	7.3198	222.174483	8.6680
s349	183.5949	32.2510	206.000	32.6680

The tabular column shows the test overhead for ISCAS-89 bench mark circuits. It presents information in terms of over consumption in power and area when scan stitching is done. The bench mark circuits have been synthesized using Synopsys DFT Compiler tool using UMC 90 nm library.

Bar chart area report:



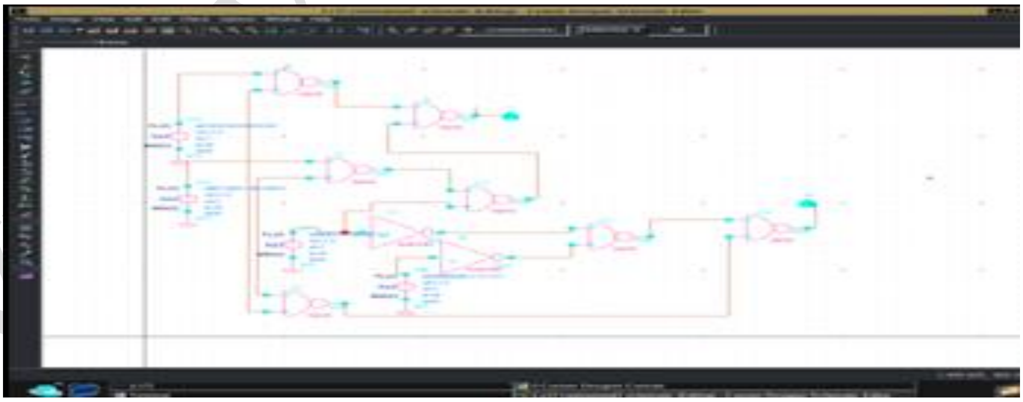
The bar chart presents information about the difference in area before and after the scan insertion.



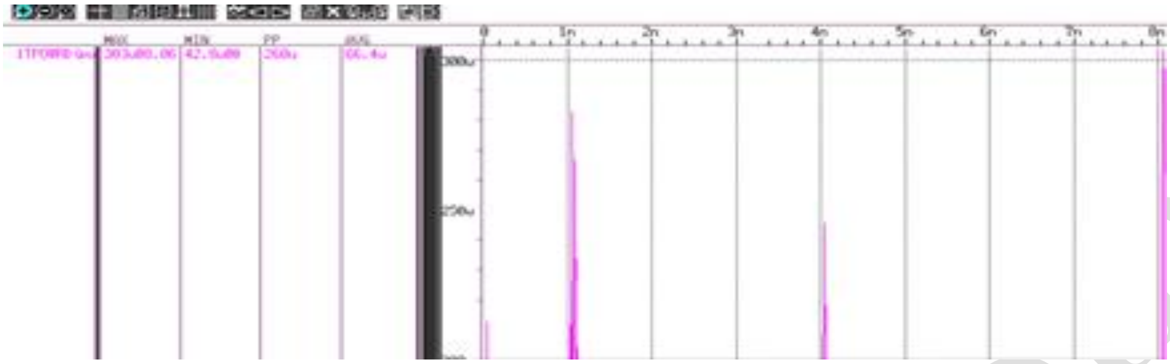
The bar chart presents information about the difference in power consumption by the ISCAS 89 circuits before and after the scan insertion.

B. Circuit diagram

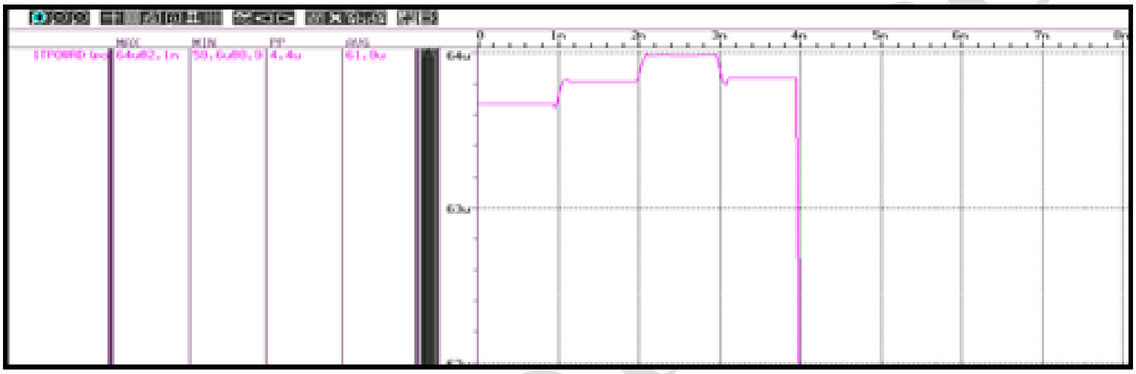
The snap shot shows s27 bench mark circuit which has been drawn using Synopsys Custom Designer tool. The bench mark circuits were drawn using the Custom Designer tool in order to estimate the power consumption by the circuits during testing.



The snap shot shows c17 bench mark circuit which has been drawn using Synopsys Custom Designer tool. The bench mark circuits were drawn using the Custom Designer tool in order to estimate the power consumption by the circuits during testing.



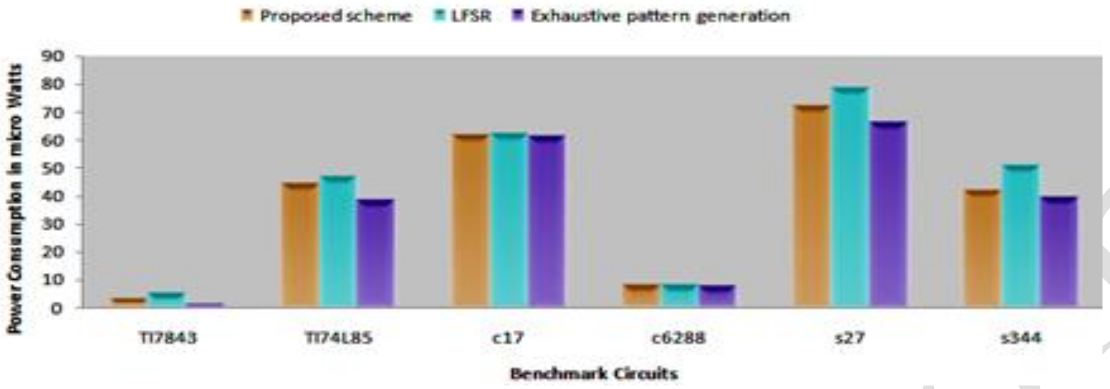
The snap shot shows the power report ofs27 bench mark circuit .Further, the bench mark circuits were drawn using the Custom Designer tool in order to estimate the power consumption by the circuits during testing.



The snap shot shows the power report of c17 bench mark circuit. Further the bench mark circuits were drawn using the Custom Designer tool in order to estimate the power consumption by the circuits during testing.

S.NO	BENCHMARK CIRCUITS	EXHAUSTIVE PATTERN GENERATION METHOD	LFSR	PROPOSED SCHEME
1	TI7843	3.12µW	5.39µW	1.1µW
2	TI74L85	44.3µW	46.9µW	38.3µW
3	C17	61.9µW	62.4µW	61.5µW
4	C6288	8.12mW	8.34mW	7.79mW
5	S27	72mW	78.6mW	66.4mW
6	S344	42µW	51µW	39.4µW

The tabular column shows the power consumption of bench mark circuits. For the considered above circuits the proposed scheme shows reduction in the average power consumption. Regardless of the fact that ISCAS 85 circuits have a bit lower reduction in average power consumption, ISCAS 89 depicts a drastic down fall in average power consumption. The same has been plotted in bar chart which is shown below.



VII. CONCLUSION

This paper has proposed a method to improve the existing standard of deriving MSIC sequences and the proposed standard is highly versatile in hardware implementation. The test patterns that are derived from the stated design are not only consumes less power during testing but also improves the fault coverage by taking less time to attain it. Here, using Vector re-ordering algorithm to improve the performance is just an initiative .There are more scrupulous algorithms in literature which is more efficient than Vector re-ordering algorithm are available to produce further optimization. In future by combining one more algorithms with the existing module could lead to achieve more efficient optimization with trade off.

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