

# RECONFIGURABLE FAST FILTER BANK FOR MULTI-STANDARD WIRELESS RECEIVERS USING MFT-VDF

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**Abstract**— A multi-standard wireless receiver (MSWR) enables different air interfaces to be implemented on a single generic hardware platform by replacing conventional analog signal processing with the digital signal processing. Operations such as spectrum sensing and channelization for MSWRs are usually performed using a filter bank. The filter bank must be dynamically reconfigurable with minimum hardware overhead to support multiple communication standards with different channel bandwidth and center frequency specifications. Moreover, the filter bank should be hardware-efficient in terms of area and power. This brief presents a new low-complexity reconfigurable fast filter bank (RFFB) using a MFT-VDF for wireless communication receivers which is efficient than the available RFFB in terms of area and complexity. We have implemented the efficient MFT-VDF architecture for designing a VDF that can be reconfigured as a low pass, high pass, band pass and band stop filter.

**Keywords**— FFB, VDF, VHDL, FPGA

## I. INTRODUCTION

In a typical multi-standard wireless communication receiver, different air interfaces to be implemented on a single generic hardware platform by replacing conventional analog signal processing with the digital signal processing. The RFFB allowed fine control of the sub-band bandwidths and their center frequencies. In RFFB, the bandwidth and center frequency of sub-bands can be varied with high frequency resolution without hardware reimplementations. This is achieved with an improved modified frequency transformation-based variable digital filter (MFTVDF) at the first stage of the proposed multistage implementation. Variable digital filters (VDFs) are digital filters with controllable spectral characteristics such as variable cut-off frequency response, adjustable pass band width, controllable fractional delay, etc. They found applications in different areas of signal processing and communications.

A number of different filter bank design approaches are available. The discrete Fourier transform filter bank (DFTFB) is a modulated filter bank that consists of a low-pass prototype filter followed by DFT operation [1] and widely used for various communication applications. However, DFTFBs have the drawbacks of uniform sub-band bandwidth and fixed center frequency for each sub-band. An improved DFTFB using coefficient decimation method (CDM) has been proposed in [2] which allows changing sub-band bandwidths using a fixed-coefficient filter at low reconfiguration overhead. However, it provides only coarse control over sub-band bandwidth because the decimation factor in the CDM is restricted to be integers. Also, center frequency of sub-bands in CDM-DFTFB is fixed. Low-complexity, reconfigurable filter banks based on frequency response masking and CDM for MSWRs are proposed in [3] and [4]. As the decimation and interpolation factors are limited to integer values, a fine control over the bandwidth is difficult to achieve using these filter banks.

The fast filter bank (FFB) is a low complexity alternative to DFTFB [5] and is suitable for applications requiring sharp transition bandwidth (TBW). However, the FFB in [5] has the same drawbacks as that of DFTFB, i.e., the inability to provide non-uniform bandwidth sub-bands and the constraint of fixed center frequency for each sub-band. Further extensions and improvements of FFBs have been suggested in [6] and [7]. In particular, multi-resolution FFB in [7] provides coarse control over sub-band bandwidth by changing the filter bank resolution. However, all filter banks mentioned above fail to provide fine control over the bandwidth and center frequency of sub-bands.

A new approach of reconfigurable filter bank design by combining FFB and a variable digital filter (VDF) is proposed [8]. First, a modified second-order frequency transformation-based low-pass VDF (MFT-VDF) that offers wide cut-off frequency range than existing VDFs is proposed. Then, the proposed reconfigurable FFB (RFFB) is designed by replacing fixed-coefficient low-pass sub-filter in the first stage of FFB with the MFT-VDF. The RFFB provides fine control over the sub-band bandwidth on the desired bandwidth range. This makes RFFB suitable for MSWRs where wideband input signal consists of channels of distinct bandwidths. However it is not efficient in terms of area and complexity. Moreover a new low-complexity reconfigurable fast filter bank (RFFB) using a MFT-VDF for wireless communication receivers which is efficient than the available RFFB in terms of area and complexity is proposed. We have implemented the efficient MFT-VDF architecture for designing a VDF that can be reconfigured as a low pass, high pass, band pass and band stop filter.

The rest of this brief is organized as follows. The design details of VDFs are provided in Section 2 followed by design of the RFFB in Section 3. A design example and gate count complexity comparisons are shown in Section IV and Section V respectively. Finally, Section VI concludes this brief.

## II. REVIEW OF VDFS

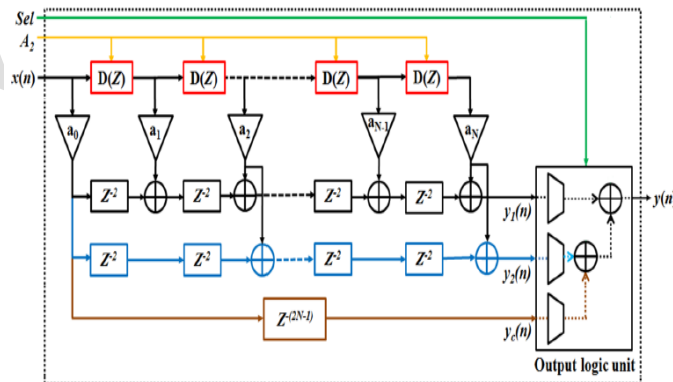
VDF is a filter whose frequency specifications such as cut-off frequency,  $f_c$ , phase delay or group delay can be controlled through a small number of parameters with minimum overhead on complexity. For the proposed RFFB, a linear phase VDF that offers unabridged control over  $f_c$  on a wide frequency range is desired. A number of linear phase VDF designs are available in literature [4], [9]–[11]. A programmable filter [9] cannot provide an efficient solution due to the large memory and reconfiguration time required. CDM-VDF in [4] fails to provide unabridged control over  $f_c$  on a wide frequency range. Farrow structure based VDFs [10],[11] have higher gate count complexity when  $f_c$  needs to be varied over a wide frequency range. Hence, we shall concentrate on frequency transformation-based VDFs.

Consider a causal linear phase FIR filter  $H(z)$  of order  $2N$  with symmetric coefficients which will be referred to as the prototype filter. This prototype filter can be implemented in Taylor form by expressing the transfer function as

$$H(z) = \sum_{n=0}^N a_n z^{-N} \left[ \frac{z + z^{-1}}{2} \right] \quad (1)$$

where the coefficients are related to the impulse response coefficients of  $H(z)$ , through the Chebyshev polynomials. The second-order transformation is given by

$$\frac{z + z^{-1}}{2} = \sum_{k=0}^n A_k \left( \frac{Z + Z^{-1}}{2} \right)^k \quad (2)$$



(a)

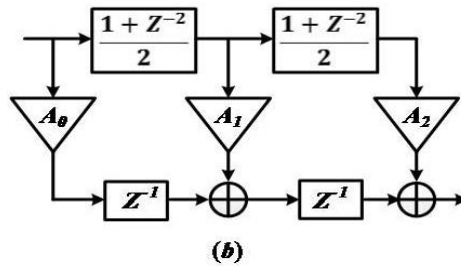


Fig.1. (a) VDF . (b) Second-order frequency transformation, D(Z).

where parameters are the transformation coefficients which controls the relationship between  $H(z)$  and second-order transformation based VDF,  $H_2(Z)$ . Substituting (2) in (1), we obtain the transfer function , as

$$H_2(Z) = \sum_{n=0}^N a_n Z^{-2(N-n)} \underbrace{\left[ \sum_{k=0}^2 A_k Z^{k-2} \left( \frac{1+Z^{-2}}{2} \right)^k \right]^n}_{D(Z)}. \quad (3)$$

Let and be the cut-off frequencies of  $H(z)$  and , respectively. Substituting and in (2), we get

$$\cos \omega_c = \sum_{k=0}^2 A_k (\cos \Omega_c)^k \quad (4)$$

From (4), the and TBW of are given by

$$\Omega_c = \cos^{-1} \left( \frac{-A_1 \pm \sqrt{A_1^2 - 4A_2(A_0 - \cos \omega_c)}}{2A_2} \right) \quad (5)$$

$$TBW = \left( \frac{A_1 \sin \Omega_c + A_2 \sin 2\Omega_c}{\sin \omega_c} \right) \quad (6)$$

if the following constraints are met :

$$A_0 + A_1 + A_2 = 1 \quad (7a)$$

$$0 \leq A_1 \leq 1 \quad (7b)$$

$$A_1^2 - 4A_2(1 - A_1 - A_2 - \cos \omega_c) \geq 0 \quad (7c)$$

The implementation of is shown in Fig. 1(a), where second-order transformation is realized through  $D(Z)$  shown in Fig. 1(b). The cut-off frequency and TBW of are controlled through the parameters, , and . is set to unity in order to reduce the number of multipliers and number of variable parameters. However, by restricting to unity, the range over which the cut-off frequency can be varied is limited to approximately 12.5% of the sampling frequency through empirical observations.

This in turn results in limited control over the sub-band bandwidth of the filter bank. For MWCR applications, wide and high frequency resolution control over sub-band bandwidth is required to extract the channels corresponding to different communication standards. The motivation behind the proposed work is to improve the area of the VDF while maintaining a low implementation complexity.

The most commonly used forms of a filter are Low pass, High pass, Band pass, and band stop. The work proposed in the paper is further expanded by utilizing the MFT-VDF architecture for implementing a variable digital filter that can be used for all the four vital configurations of a filter (Low pass, High pass, Band pass and Band stop) and the corresponding response of each filter configuration is obtained. The switching between the different configurations is made possible by use of a simple select line and output logic unit so that the same VDF can be reconfigured to obtain any of the four filter responses. The MFT-VDF is then incorporated in a Reconfigurable Fast Filter Bank (RFFB).

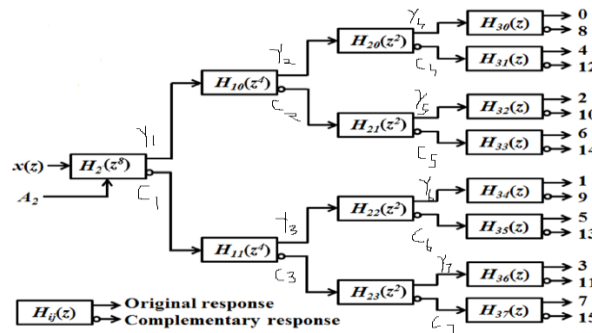


Fig.2. Proposed RFFB

### III. PROPOSED RECONFIGURABLE FAST FILTER BANK

The RFFB is designed to provide fine control over the sub-band bandwidth. Let the design specifications of the RFFB with  $L$  sub-bands be: minimum and maximum sub-band bandwidth as  $\omega_{min}$  and  $\omega_{max}$ , respectively, desired TBW as  $\omega_{TBW}$ , pass-band ripple as  $\delta_p$ , stop-band attenuation as  $\delta_s$ . All the frequency specifications mentioned here are normalized with respect to half the sampling frequency. The structure of the RFFB with  $k = M$  stages is shown in Fig. 2, where  $M$  is the interpolation factor for the first stage and equal to  $L/2$ . The RFFB design is described in detail below.

#### A. First Stage – VDF

The low-pass VDF in the first stage is designed using modified second-order frequency transformation with transfer function  $D(Z)$  in the form given by (3). The range over which cutoff frequency of  $\omega_c$  can be varied is decided by parameters  $A_1$  and  $A_2$ , while the order of the prototype filter of is  $N$  decided by its TBW, pass-band ripple, and stop-band attenuation specifications. Expanding  $D(Z)$  in (3), we have

$$D(Z) = A_0 Z^{-2} + A_1 Z^{-1} \left( \frac{1 + Z^{-2}}{2} \right) + A_2 \left( \frac{1 + Z^{-2}}{2} \right)^2 \quad (8)$$

From the constraints given by (7), we have  $A_0 = 1 - A_1 - A_2$ . Substituting  $A_0$  into (8) and simplifying, we obtain

$$D(Z) = A_1 \left[ \left( \frac{Z^{-1} + Z^{-3}}{2} \right) - Z^{-2} \right] + Z^{-2} - A_2 \left[ Z^{-2} - \left( \frac{1 + Z^{-2}}{2} \right)^2 \right] \quad (9)$$

In this way, only two multipliers are needed instead of three multipliers, to implement  $D(Z)$ .  $A_0$  is fixed to unity. In the proposed MFT-VDF, we have relaxed the constraint that  $A_1 = 1$  so that  $A_2$  allows a much wider cutoff frequency range. The design steps for the first stage of RFFB are as follows.

- 1) Based on desired  $\omega_c$  and  $\Omega_c$ , the lower and upper cut-off frequencies of  $H_2(Z)$ ,  $fc_1$  and  $fc_2$ , respectively, are calculated as  $M/2$  times  $\omega_c$  and  $\Omega_c$ , respectively.
- 2) For a desired range from  $\omega_c = (2\pi fc_1)$  to  $\Omega_c = (2\pi fc_2)$ , corresponding value of  $A_1$  and range of  $A_2$  are calculated using (5)–(7). This is an iterative procedure where for a given  $A_1 (0 \leq A_1 \leq 1)$  and  $\omega_c$ , corresponding range of  $A_2$  and  $\Omega_c$  are obtained using (7) and (5) respectively. Note that  $A_1 (0 \leq A_1 \leq 1)$  is fixed and restricted to sum of reciprocals of power-of-two values to keep the multiplier complexity same. In case where multiple combinations of  $\omega_c$ ,  $A_1$ , and  $A_2$  provide same cut-off frequency range from  $\omega_c$  to  $\Omega_c$ , the set which provide better TBW performance as per (6) is selected in order to reduce the order of the MFT-VDF,  $H_2(Z)$ .
- 3) The maximum pass-band ripple and minimum stop-band attenuation of the prototype filter of  $H_2(Z)$  are equal to  $\delta_p$  and  $\delta_s$ , respectively.
- 4) As the TBW of the  $H_2(Z)$ , is not constant over the frequency range from  $fc_1$  to  $fc_2$  as shown in (6), TBW<sub>0</sub> of the prototype filter of  $H_2(Z)$  is chosen such that the maximum TBW over the range  $fc_1$  to  $fc_2$  is equal to or narrower than  $M^*$ .
- 5) Based on these parameters  $\omega_c$ ,  $\Omega_c$ ,  $A_1$ , and  $A_2$ , is designed as discussed in Section II and interpolated by  $M$  to get multiband original ( $O_1$ ) and complementary ( $C_1$ ) responses.

For the desired  $\omega_c = 2\pi fc$ , corresponding value of  $A_2$  can be obtained by rewriting (4) as

$$A_2 = \left( \frac{\cos \omega_c - A_0 - A_1 \cos \Omega_c}{(\cos \Omega_c)^2} \right) \quad (12)$$

In this way, by controlling  $\omega_c = 2\pi fc$  of  $H_2(Z)$  using  $A_2$ , fine control over sub-band bandwidth from  $BW_{min}$  to  $BW_{max}$  is achieved. Furthermore, by combining adjacent sub-bands and varying  $A_2$ , RFFB offers fine control over center frequency of fixed bandwidth sub-bands.

### B. Remaining Stages – Fixed-Coefficient Digital Sub-Filters

The remaining stages of the RFFB consist of fixed coefficient sub-filters,  $H_{ij}(z)$ , where  $1 \leq i \leq (k-1)$  and  $0 < j \leq (2i-1)$ , arranged in a tree structure similar to uniform FFB [6] as shown in Fig. 2. The design steps for remaining stages are as follows.

- 1) The  $(k-1)$  sub-filters,  $H_{i0}(z)$ ,  $1 \leq i \leq (k-1)$  and  $j = 0$  are fixed-coefficients even-order low-pass filters which shall be known as sub-prototype filters. The cut-off frequency of all these sub-prototype filters is fixed and equal to 0.5 in the normalized frequency scale. The  $\delta_p$  and  $\delta_s$  of the filter bank and all sub-prototype filters are kept same

- 2) The transition bandwidths of the sub-prototype filters,  $H_i(z)$ ,  $1 \leq i \leq (k-1)$ , are given by

$$TBW_i = 1 - \left( f_{c2} + \frac{TBW_d}{2} \right) 2^{(1-i)} \quad (13)$$

where  $f_{c2}$  is maximum cut-off frequency of the .

- 3) Based on these parameters,  $H_i(Z)$ , where  $1 \leq i \leq (k-1)$ , are designed and then interpolated by the factor  $M/2i$ .
- 4) The remaining sub-filters, , where  $1 \leq i \leq (k-1)$  and  $1 \leq j \leq (2i - 1)$ , are obtained by modulating the corresponding interpolated sub-prototype filters,  $H_i(Z(M/2i))$ .

The RFFB differs from the uniform FFB [6] in the following aspects: The sub-band bandwidth in the  $L$ -sub-band uniform FFB [6] is fixed and equal to  $(2/L)$ . The RFFB with MFT-VDF in the first stage, provides uniform bandwidth sub-bands of bandwidth  $(2/L)$  as well as non-uniform bandwidth sub-bands with bandwidth varying from to , where  $( \leq (2/L) \leq )$ . It can be observed from (10) and (11) that higher the value of  $f_{c2}$  ( $=fc$ ), wider is the range over which sub-band bandwidths can be varied. As  $f_{c2}$  is inversely proportional to TBW according to (13), wider sub-band bandwidth variation range comes at the cost of narrow TBW sub-filters in remaining  $(k-1)$  stages. As the  $f_{c2}$  in the proposed RFFB is higher than that in uniform FFB [6], where  $f_{c2} = 0.5$ , the fixed-coefficient sub-filters in the remaining stages of our RFFB have narrow TBWs (which means higher order, i.e., more gate count complexity) than that of the uniform FFB in [6] for a given  $TBW_d$ ,  $\partial p$ , and  $\partial s$  . This is the penalty in terms of number of gate counts incurred while achieving fine control over sub-band bandwidths. As  $H_2(Z)$  is a linear phase VDF and all sub-filters in remaining stages have linear phase, the RFFB retains the linear phase property of the FFB in [6] which is required for most of the communication applications.

#### IV. HARDWARE IMPLEMENTATION AND DESCRIPTION

The on-repeating patterns generated are shown below in the display of FPGA kit. Here SPARTAN3 kit is used for the implementation. FPGA is a predesigned reconfigurable IC. It can be reconfigured any number of times according to the specification of design. Field Programmable Gate Arrays (FPGAs) are emerging as an attractive platform for random number generator implementations.

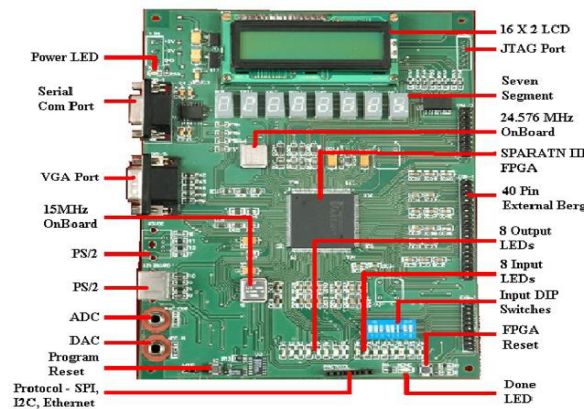


Fig.3. FPGA-Spartan3 Kit



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