



A DYNAMIC RECONFIGURABLE FIR FILTER FOR SDR APPLICATIONS

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Abstract: The everlasting growth of VLSI technology makes the communication device as compact as possible in case of both area and power. Especially in mobile platform, the area of transceivers is reduced, in which filters are used for pulse shaping, matched filtering, and channel equalization. The filters used in mobile communication must employ two important properties such as reduced power consumption and higher operational speed. Recently emerged technology called as Software Defined Radio (SDR) is capable of supporting most of the available and advanced wireless standards in telecommunication industry. It consists of digital Finite Impulse Response (FIR) filters for its digital up conversion and down conversion blocks. SDR technology focuses mainly on reconfigurability, where the coefficients need to be dynamically programmable in real time and the length of the filter may vary according to the computing platform. The multiplier plays vital role in defining the performance of the desired filter. Numerous algorithms are available for implementing the multiplier architecture. Existing systems have efficient constant multiplier architecture to realize reconfigurable FIR filter. The proposed FIR filter multiplier architecture is capable of operating for dynamically varying filter coefficients without any overhead in the hardware circuitry. Here, I use binary common sub expression elimination algorithm in initial stages to eliminate redundancy in filter coefficients. To improve the reconfigurability of a FIR filter, BCSE algorithm can be applied in both vertical and horizontal directions. Thus, a highly dynamic reconfigurable FIR filter can be realized with reduced hardware complexity. The proposed approach results in low cost and high speed multiplier with reduced power, delay and area compared to existing technology.

Keywords: Binary Common Sub expression Elimination, Finite Impulse Response, Vertical Horizontal Binary Common Sub expression Elimination, Software Defined Radio.

I. INTRODUCTION

A. OVERVIEW OF THE PROJECT

The main requirement of telecommunication industry nowadays is a high data transfer and high channel capacities. In an SDR system, multiple standards can be realized in a single chip by providing a programmable channel select filter at the baseband level. Low pass interpolation filter can be used in transmitter side to boost the baseband input sampling frequency. Similarly, low pass decimation filter can be used in receiver side to control the bandwidth. Because of different channel bandwidths, carrier-to-noise ratios, blocking, and interference problems, there is a need of reconfigurable channel filter for data rate conversion. Several researches can be done in designing a low power, low area, and low complexity reconfigurable FIR filter. The FIR filter can be realized in two different forms such as direct form and transposed form. The direct form realization of FIR filter is represented by the below equation as

$$y_n = \sum_{k=0}^{n-1} h_k x_{n-k} \quad (1.1)$$

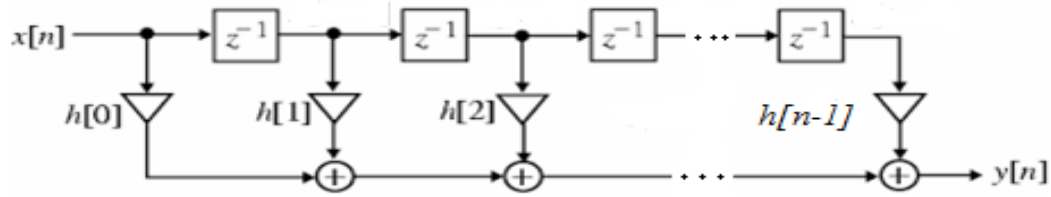


Fig. 1 Direct form realization of FIR filter.

It consists of three major blocks such as multiplication, addition, and unit delay. The major constraints in determining the desired performance of the FIR filter is the multiplier block. In FIR filter, the multiplication operation is performed between one input variable and many constants and is called as Multiple Constant Multiplication (MCM). For fixed point FIR filter realization, the algorithms introduced for efficient multiplier implementation can be categorized as graph based algorithm and Common Sub-expression Elimination (CSE) algorithm. But for SDR applications, the filter coefficient can be dynamically changed in real time. Binary Common Sub-expression Elimination (BCSE) algorithm is one of the techniques useful to obtain reconfigurable FIR filter with low complexity. The choice of the BCS length is fixed and also the input and coefficients are represented in signed magnitude format provides a way for defining new algorithm called as VHBCSE, where signed decimal representation is used.

II. LITERATURE SURVEY

Numerous algorithms were reported in published literatures for implementing efficient multiplier architecture for fixed point FIR filter. For constant multiplication operation, two algorithms were proposed earlier and they were graph based algorithms [1] and common sub expression elimination(CSE) algorithm [6]-[11]. Graph theoretical methodology [1] was available to reduce the hardware complexity in multiplication operation for implementing FIR filter. A combination of CSE algorithm and shift inclusive differential coefficients to improve the cost of the solution. For multistandard wireless receivers [2] fast filter banks were used to obtain low complexity reconfigurable FIR filter and it mainly focuses on spectrum sensing and channelization applications. A 2-bit BCSE algorithm [3] and 3-bit BCSE algorithm [6] was proposed earlier to implement efficient constant multiplier architecture. Due to the fixed bit BCSE algorithm, the redundant computation can be vertically eliminated across the adjacent coefficients only in first layer and then the adders, which results in high power consumption at the lower level. For wide applications, signed decimal data representation is mostly used but this technique uses signed magnitude number format for input as well as the coefficient. Partitioning algorithm [11] focused on reducing the number of adders needed to implement the coefficient multipliers. In case of common sub expression elimination technique, by means of reduction in number of adders and critical path, low complexity multiplier can be achieved. But this algorithm achieves low complexity and high speed by reducing the complexity of each adder. A new common sub expression elimination algorithm [5] introduced a new CSE algorithm for the implementation of higher order FIR filters in which coefficients are represented in binary form. In the existing, filter implementation Canonical Signed Digit (CSD) based CSE method reduces the number of adders required for multiplier. The proposed binary coefficient based CSE method have good reduction in the number of adders in realizing higher order filters. Without increase in the critical path length of filter coefficient multiplier can be achieved here. On analysing the above published literatures, a new algorithm to realize reconfigurable efficient constant multiplier will be proposed here.

The organization of the paper is as follows. In section III, basic concepts about BCSE algorithm and detailed hardware architecture of reconfigurable efficient constant multiplier will be narrated. In section IV, implementation and results of above architecture such as area, power and resource utilization has been described. Finally, the paper is concluded and also future enhancement is provided in section V.

III. RECONFIGURABLE CONSTANT MULTIPLIER

A. BCSE ALGORITHM

CSE algorithm is commonly useful to reduce the number of adders required to perform multiplication operation in FIR filter. In CSE method, generally Canonical Signed Digit representation of inputs and coefficients are used. By eliminating common sub expression in those filter coefficients the hardware complexity can be reduced. But, BCSE algorithm reduces more number of adders than CSD based CSE algorithm. This is because of lesser number of unpaired bits in binary representation than CSD

representation of filter coefficients. In BCSE algorithm, the first step is to find the Binary Common Sub expressions (BCSs) in partial products generated in multiplication operation. By means of this adder reduction, the hardware complexity and cost of multiplier can be decreased. The redundant computations within the coefficient and in the adjacent coefficient can be eliminated separately by two methods namely, horizontal BCSE algorithm and vertical BCSE algorithm respectively. By means of above two techniques, efficient multiplier architecture with reduced cost, area, and power can be easily obtained.

B. VHBCSE ALGORITHM

Vertical-horizontal BCSE algorithm can be used to implement constant multiplier for FIR filter. The designed multiplier considers the input (x) having length 16-bits and coefficient (h) having length 17-bits while the output is assumed to be 16-bit long here. VHBCSE multiplier supports the signed decimal data representation, so the sign conversion block is used here to perform the operation of both positive and negative valued coefficients. The partial products are generated using shift and add based techniques. Then, the multiplexed coefficient from the sign conversion block is used to select the proper data generated from the sign conversion block. Finally, with the help of control logic generator, the controlled addition is performed to obtain the final result.

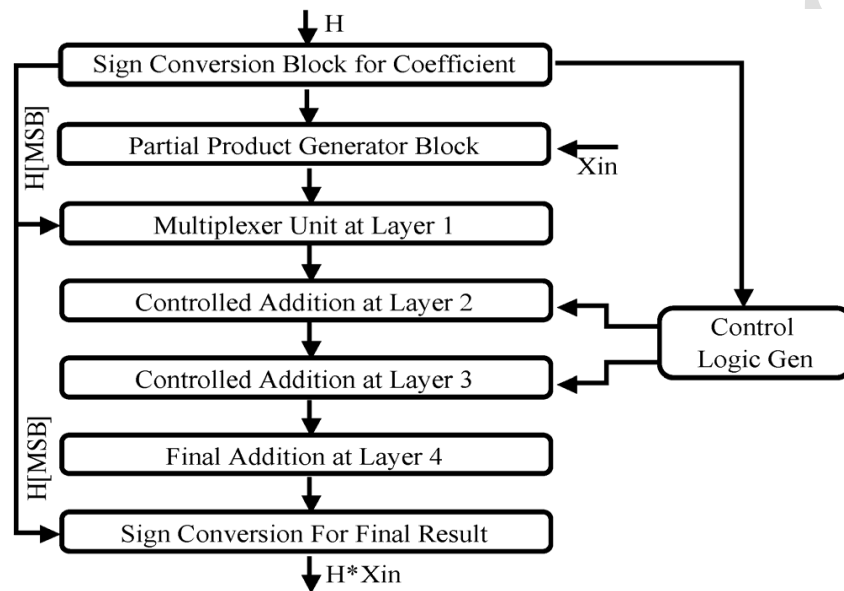


Fig. 2 Dataflow diagram of the CM using VHBCSE algorithm

C. HARDWARE ARCHITECTURE OF RECONFIGURABLE CONSTANT MULTIPLIER

The hardware architecture of VHBCSE multiplier consists of different blocks to perform the multiplication operation in FIR filter mainly useful for SDR applications. They are:

- Sign Conversion Block.
- Partial Product Generation.
- Multiplexers unit.
- Control Logic Generator.
- Controlled addition at layer-2.
- Controlled addition at layer-3.
- Final addition on layer-4.

- 1) *Sign Conversion Block:* Sign conversion block is used here to support both the input and the coefficient representation in signed decimal data format. To generate the inverted version of the 16-bit coefficient, 1's complement block is present here. Depending on the most significant bit of coefficient value, 2:1 multiplexer produces the multiplexed coefficients. For negative value of the original coefficient, the multiplexed coefficient value will be in inverted form otherwise, it will be as above.
- 2) *Partial Product Generation:* Shift and add based technique is used to generate the partial product. The number of partial products depends on the size of BCSs used. Here, 2-bit BCSs ranging from "00" to "11" are used. In above four BCSs,

a single adder will be required for the pattern “11”. The remaining partial products are generated by hardwired shifting. For the coefficient of 16-bit length, 8 partial products of 17, 15, 13, 11, 9, 7, 5, and 3 bits (P1-P8) can be obtained. By means of above method, the size of multiplexers used in the next will be reduced significantly.

- 3) *Multiplexers Unit:* The multiplexers unit works based on the multiplexed coefficient from the sign conversion block. It is used to select the appropriate data from PPG unit. To do so, eight 4:1 multiplexers are required. It produces the final partial products according to the 2-bit BCSE algorithm applied vertically on the coefficients. The width of these eight multiplexers are 17, 15, 13, 11, 9, 7, 5, and 3-bit, which reduce the hardware complexity and power consumption compared to the conventional 16-bit multiplexers.
- 4) *Control Logic Generator:* The multiplexed coefficient from the sign conversion block is used as the input to generate control signals for controlled addition at layer-2 and layer-3. Totally, 7 control signals have been generated with the help of comparator blocks. Here, the multiplexed coefficients are partitioned into two groups, one having 4-bits each and another one having 8-bits each for 4-bit and 8-bit equality check. For simplicity, the control signals generated from 4-bit comparator will be used for 8-bit equality check.
- 5) *Controlled Addition at Layer-2:* The partial products from the multiplexer unit are added up to obtain final multiplication result. This addition operation can be done in 3-layers one by one. First of all, to sum up eight PPs, four adders are required to perform addition (A1-A4) operations. Different from BCSE, this algorithm uses control signals from the control logic generator block to perform controlled addition at this layer. The control signals (C1-C6) generated based on 4-bit BCSE are used here. From the below architecture, the propagation delay at this layer is maximum between the paths used to generate AS2, AS3 and AS4.
- 6) *Controlled Addition at Layer-3:* In this layer, four multiplexed sums (AS1, AS2, AS3, and AS4) from layer-2 are summed up by means of two adders. In these two adders, A6 can be controlled using control signal C7 generated from control logic generator block based on 8-bit BCSE. Here, the propagation delay present in the path used to generate AS6.
- 7) *Final Addition on Layer-4:* The addition operation between the two sums (AS5, AS6) from the above layer is produced in this block. It is used to generate the final multiplication result between the input and the coefficient.

The block diagram of the over-all constant multiplication is shown in the below fig.

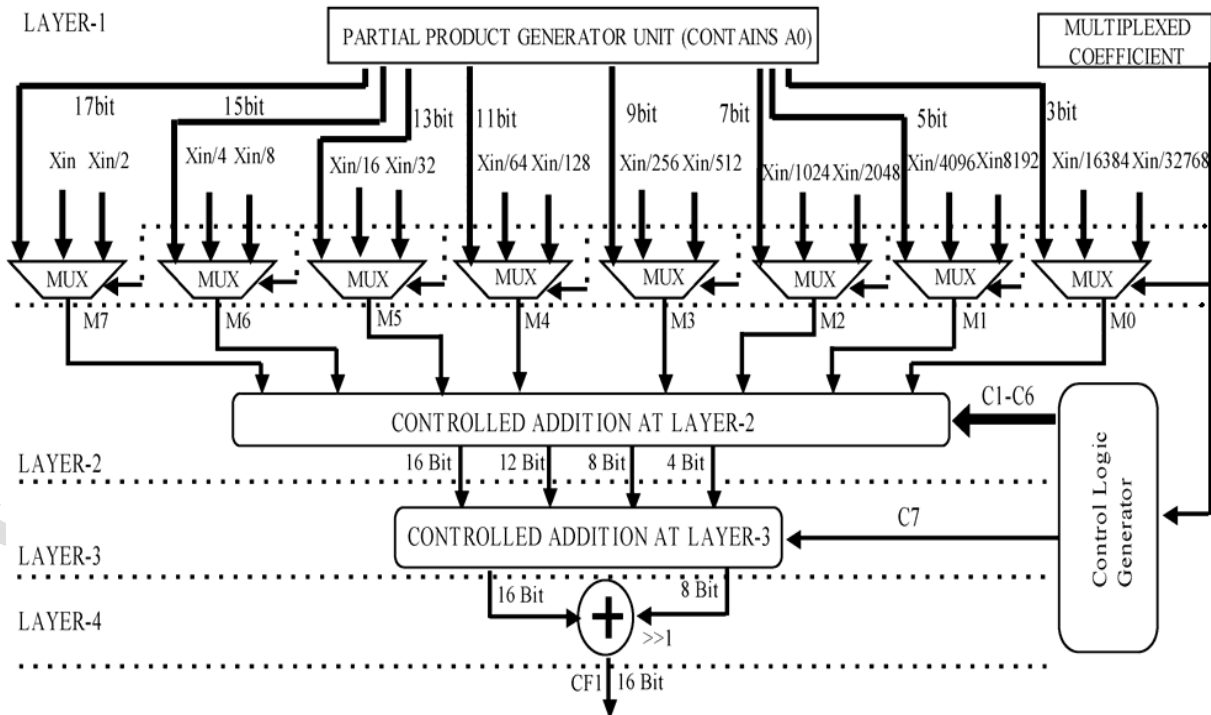


Fig. 3 Reconfigurable Constant Multiplier Architecture

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. IMPLEMENTATION

Efficient constant multiplier architecture for reconfigurable FIR filter based on VHBCSE algorithm is implemented using cadence software in “NC Verilog” tool. In the below table, hardware cost for various BCSE algorithms are analyzed briefly.

TABLE I
Hardware cost analysis of different BCSE Algorithms

	VHBCSE	2-Bit BCSE	3-Bit BCSE
Adders	2(17bit)+2(16bit)+1(13bit) +2(9bit)+1(5bit)=8	2(17bit)+2(16bit)+1(13bit)+2(9bit)+1(5bit)=8	8(16bit)
Multiplexers	8(4:1 of 17, 15, 13, 11, 9, 7, 5, and 3 bit each) + 2(2:1 of 16 bit) + 1(2:1 of 12 bit) + 3(2:1 of 8 bit) + 3(2:1 of 4 bit) =17	8(4:1 of 17, 15, 13, 11, 9, 7, 5, and 3 bit each)+1(2:1 of 16 bit)=9	5(8:1 of 16 bit) +2(2:1 of 16 bit)=7
1's complement unit	1	0	0
2's complement unit	1	1	1
Comparator	6(4bit)+1(8bit)=7	0	0

B. EXPERIMENTAL RESULTS

The output of the above multiplier architecture can be obtained using the verilog HDL code in “waveform – simvision” window and is shown below

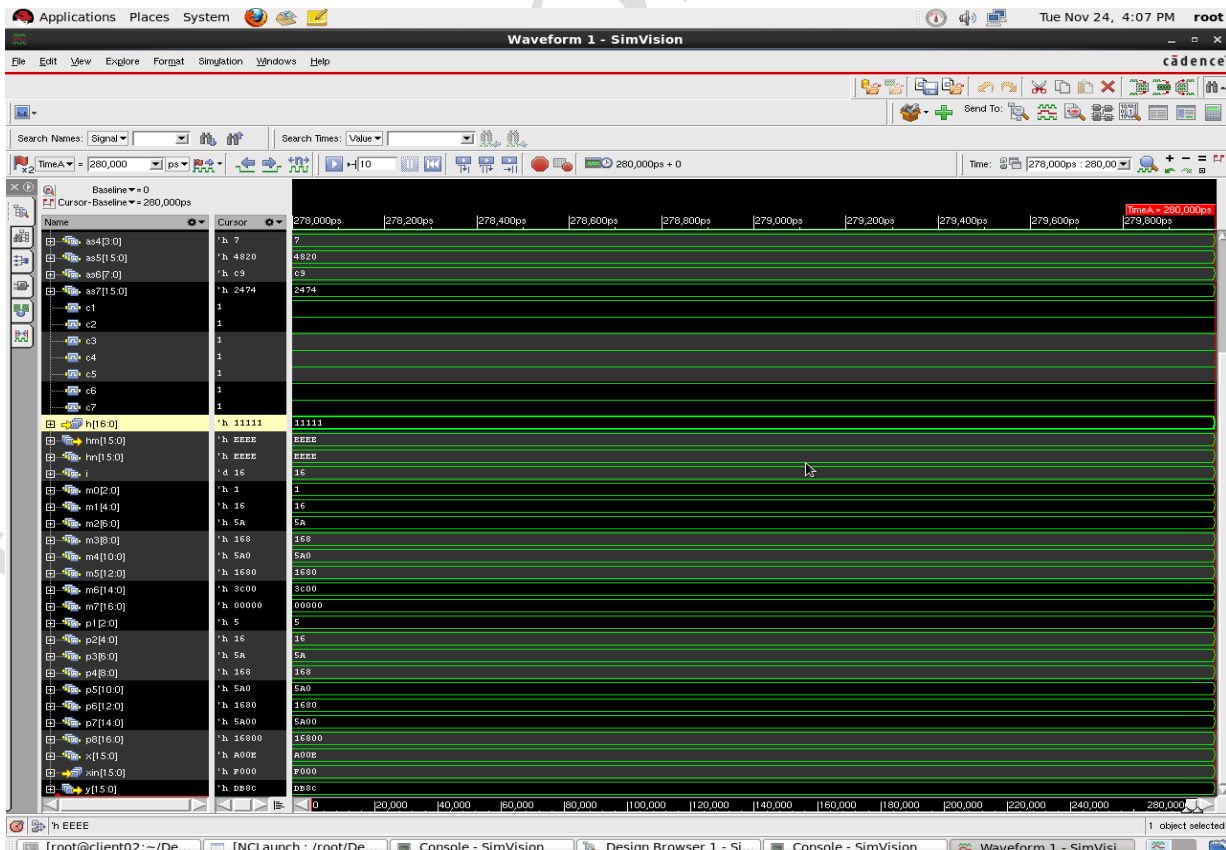


Fig. 4 Output waveform of VHBCSE multiplier

In above output waveform, the value of inputs given will be $x_{in} = 16' F000$ and $h = 17' 11111$. Then, area and power consumption of the VHBCSE multiplier architecture can be obtained by generating tcf file and early power estimation using simvision and RTL compiler and is given below.

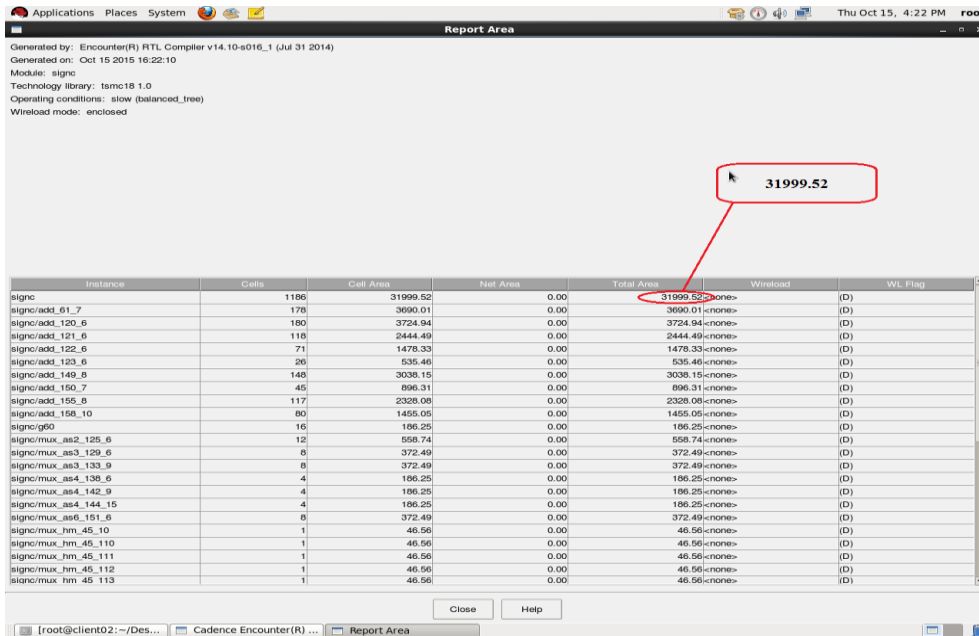


Fig. 5 Area report of VHBCSE multiplier

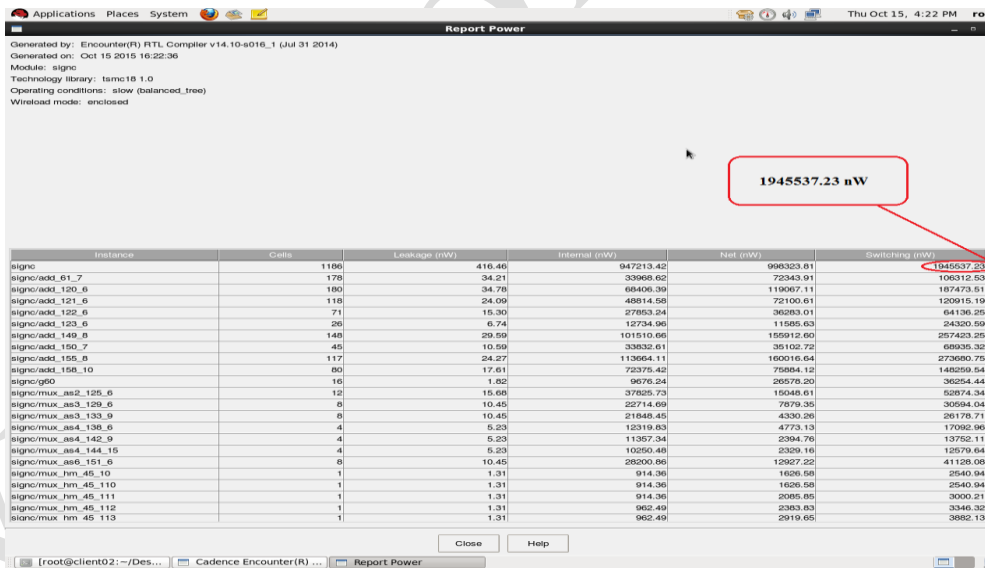


Fig. 6 Power report of VHBCSE multiplier

The schematic of VHBCSE multiplier obtained by “Encounter Digital Implementation” (EDI) tool under cadence software with the help of verilog HDL code is shown below.

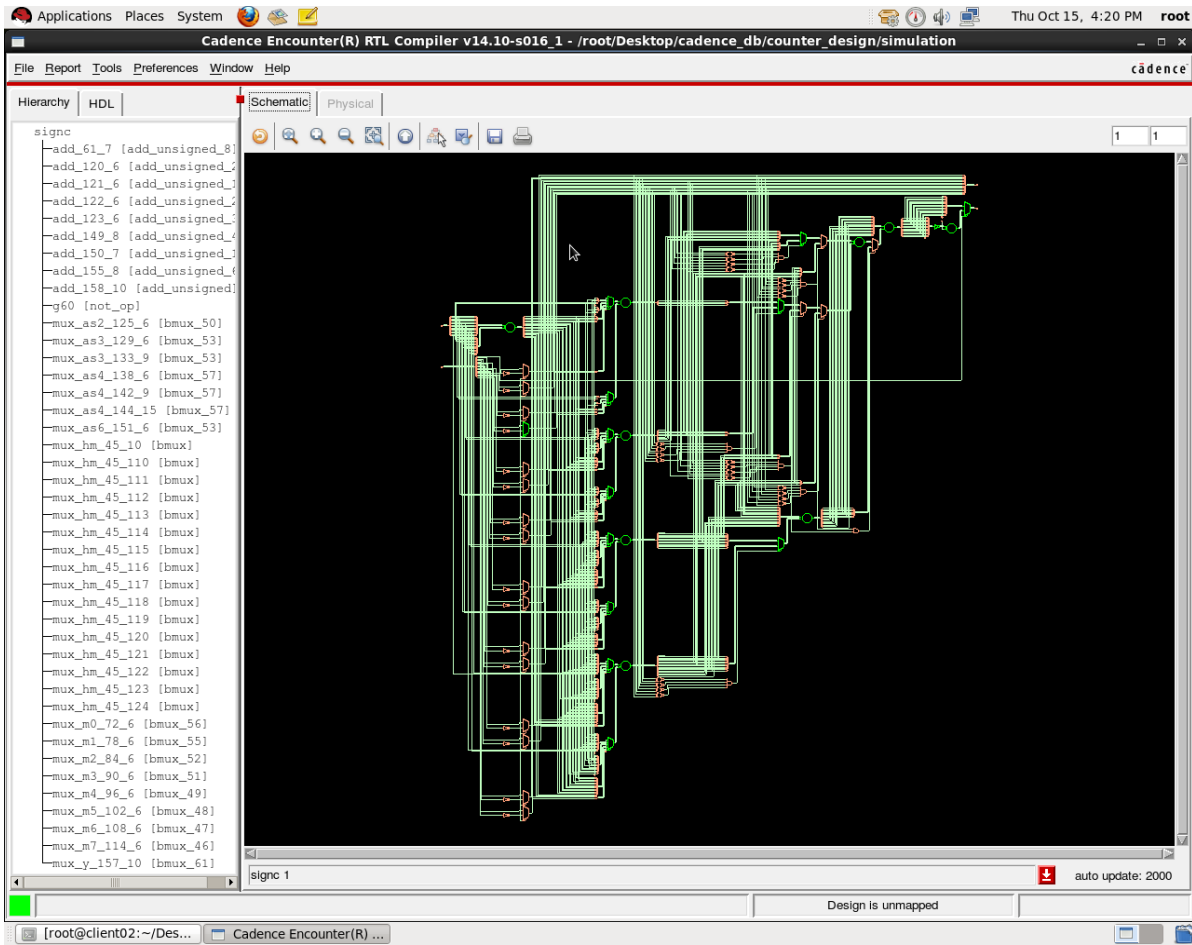


Fig. 7 Schematic of VHBCSE multiplier

After completing constant multiplier architecture using VHBCSE algorithm, the performance of above multiplier can be analysed by implementing it in the FIR filter structure. By using Xilinx ISE 9.2i synthesize tool, I analyse the operation of this reconfigurable FIR filter structure for various filter taps in the targeted FPGA device (xa3s500eftg256-4). The resource utilization of FIR filter is shown in the below table.

TABLE II
Resource utilization of 4-tap FIR filter using VHBCSE multiplier block

Resource	Used	Available	Utilization
Slice	701	4656	15%
LUTs	1321	9312	14%
Slice Flip Flops	48	9312	0%
Bonded IOBs	102	190	53%
Gclks	1	24	4%

TABLE III
Resource utilization of 20-tap FIR filter using VHBCSE multiplier block

Resource	Used	Available	Utilization
Slice	1063	4656	22%
LUTs	304	9312	3%
Slice Flip Flops	1752	9312	18%
Bonded IOBs	34	190	17%
Gclks	1	24	4%

V. CONCLUSION AND FUTURE WORK

A. CONCLUSION

To overcome the drawbacks in fixed point reconfigurable FIR filter for SDR applications, a new algorithm called VHBCSE algorithm can be proposed here. This algorithm initially eliminates the common sub expressions by applying 2-bit BCSE vertically. Afterwards, the common sub expressions within the coefficient can be eliminated by applying different length of BCSEs horizontally. Due to this, the area and power consumption reduced as compared to fixed bit BCSE algorithm. To maximize the efficiency of the multiplier architecture, signed decimal data representations are used for both input and the coefficient values of the filter.

B. FUTURE ENHANCEMENTS

The reconfiguration and efficiency of the above multiplier block can be further improved with a help of programmable shifters and also delay will be reduced in the proposed architecture to make it more suitable for SDR applications with reduced power consumption.

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