



# HIGH THROUGHPUT AND LOW POWER ASYNCHRONOUS PIPELINE STRUCTURE FOR RADIX-2 MULTIPLIER

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**Abstract:** Nowadays, most microelectronic chips (ranging from cell phones to super computers) are designed mainly based on asynchronous design, and this design avoids the global synchronization. Pipelining is a key element for the design of high-performance digital system that reduces the delay in the critical path, the speed and through-put is improved by eliminating this delay. Domino logic is very well-suited for building asynchronous circuits, which is motivating logic style for high speed and area efficient design because of its reduced number of transistors, reduced fan-in capacitance, and faster switching thresholds. A novel design method of asynchronous domino logic pipeline focuses on improving the circuit efficiency and making asynchronous domino logic pipeline design for a wide range of applications. The novel design method combines the benefits of an area-efficient and ultra-low power asynchronous domino logic pipeline. Here, the data path is composed of a mixer of dual-rail and single-rail domino gates. The dual-rail domino gates are limited to construct a stable critical data path and the single-rail domino gates are applicable for non-critical data path. For evaluating the asynchronous domino logic pipeline based on constructed critical data path, a radix-2 multiplier is used. This will be compared with other pipeline techniques such as bundled data asynchronous domino logic pipeline and synchronous pipeline with clock gating.

**Keywords:** Asynchronous domino logic pipeline, Critical data path, Single-rail domino logic gate, Dual-rail domino logic gate, Radix-2 multiplier.

## I. INTRODUCTION

### A. OVERVIEW OF THE PROJECT

Nowadays, the semiconductor industry is giving serious concern to the adoption of asynchronous circuit technology, along with the continued CMOS technology scaling. The physical-design concerns such as global clock tree synthesis and top-level timing optimization develop serious problems. Therefore the asynchronous technology uses local handshake instead of externally supplied global clock. Asynchronous circuits avoid problems related to global clock and it has greater potential for high-speed, low-power, low EMI, and a natural match with heterogeneous system timing [1], [3]. The asynchronous circuit implementations are divided into two types depends on its encoding scheme:

- Bundled-data asynchronous circuit (single rail)
- Dual-rail asynchronous circuit

Pipelining is a crucial element in the design of high-performance digital system. A domino logic data path is common in high-performance digital systems and also provides the benefits of reduced chip area higher signal transition speed and lower power consumption. Therefore the domino logic is a good match for 4-phase dual-rail protocol in asynchronous circuit design.

### B. BACKGROUND

Asynchronous domino logic pipeline depends on dual-rail data paths to transfer the data and encoded handshake signals that can also entirely avoids the explicit storage elements between stages by developing the implicit latching functionality of the gates. This latch-free feature gives the benefits of reduced critical delays, smaller silicon area, and lower power consumption [7].

PS0 pipeline is a style of asynchronous domino logic pipeline based on dual-rail protocol and it can be designed based on 4-phase dual-rail protocol. Here each pipeline stage is composed of a function block and a completion detector and each function block is realized using dual-rail domino logic and each completion detector produces separate local handshake signal to control

the flow of data through the pipeline. Then these handshake signals are transferred to the precharge/evaluation control port of the previous pipeline stage. A specific complementary logic gate is built in dual-rail domino logic to solve the problem in single-rail domino logic. The problem is that the complementary logic gate causes logic overhead which consumes more power and silicon area and the most serious problem is that the detection overhead in handshake control logic and the dual-rail encoding overhead in the data path [13].

Precharge Half-Buffer pipeline (PCHB) uses quasi-delay-insensitive control circuits, which is a timing robust pipeline style. It consists of two completion detectors, one is used at the input side and another one is used at the output side. The complete cycle of proceedings for a PCHB stage is similar to that of PS0, except that PCHB stages verify it's all input bits. Because of the input completion detector, a PCHB stage does not start evaluation until all input bits are valid. This design absorbs the skew across individual bits in the data paths. Therefore this design makes PCHB more timing-robust, it causes two times handshake overhead compared to PS0. Besides, PCHB has the same logic overhead problem as PS0 [4].

The Look-ahead pipeline (LP) is a single-rail and dual-rail asynchronous pipeline style, which provide higher throughput by using variety of optimization to reduce the impact of inter stage handshaking delays. The three distinct dual-rail look-ahead pipelines are LP3/1, LP2/2 and LP2/1. The two distinct single-rail look-ahead pipelines are LP<sub>sr</sub>2/2 and LP<sub>sr</sub>2/1. To allow anticipation of critical events, early done scheme and early evaluation scheme are combinely used here. Dual rail look-ahead pipeline achieves throughput more than twice of Williams's PS0 and single rail look-ahead pipeline achieves even higher throughput. These pipelines avoids the problem of high-speed clock distribution such as clock power, management of clock skew and inflexibility in handling in varied environments multi-GHz throughput, and also avoids the problem of high speed clock. Although such design reduces the power consumption in handshake control logic, the overhead problem in function block logic remains unsolved [8].

## II. DETAILED DESCRIPTION OF ADCDP PIPELINE

### A. APCDP Pipeline

An asynchronous pipeline based on constructed critical data path (APCDP) using domino logic with the benefits of ultralow-power and high-throughput is designed, directing to latch-free and extremely fine-grain or gate-level design. The data paths are composed of mixer of dual rail and single rail domino logic gates. Here, the dual rail logic is used to construct a stable critical data path and single rail domino logic is applied in non-critical data paths. Then the problem of asynchronous domino logic pipeline such as the dual rail encoding overhead in data path and also the detection overhead in handshake control logic are reduced by this pipeline, which is based on constructed critical data path. This latch-less feature of the pipeline provides the lower power consumption, reduced silicon area, reduced transistor count, and reduced critical delays. Then the evaluation result of this APCDP pipeline is compared with bundled data pipeline and classic synchronous pipeline.

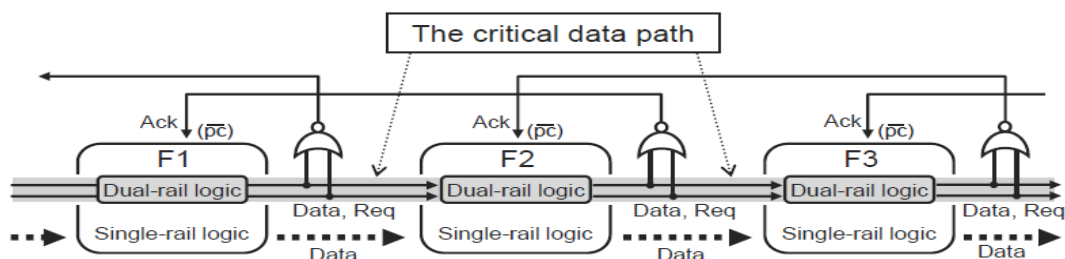


Fig. 1 Block diagram of APCDP pipeline

The asynchronous pipeline (APCDP) is designed based on a stable critical data path, which is constructed by using hybrid structure of dual-rail and single-rail logic. The block diagram of asynchronous pipeline structure is shown. The critical data path composed of dual-rail logic to transfers a data signal and an encoded handshake signal. Noncritical data path, composed of single-rail logic only transfers the data signal. The APCDP pipeline is structurally based on PS0. The difference is that the completion detector is simplified to a single NOR gate by detecting only the critical data path instead of the entire data paths. A static NOR gate detects the dual-rail critical data path and generates a total done signal for each pipeline stage. The output of NOR gates are connected to the pre charge ports of their previous stages. As a result, APCDP has a small overhead in both handshake control logic and function block logic, which can greatly, increases the throughput and power consumption. The structure of asynchronous pipeline can be divided into following modules,

- SLG (Synchronizing logic gate)

- SLGL (Synchronizing logic gate with latch function)
- S to D converter (single-rail to dual-rail converter )
- S logic (single-rail logic)

1) *SLG*: The synchronizing logic gates (SLG) are dual rail domino gates that have no gate-delay-data dependence problem by making sure that SLG cannot be activated until all inputs become valid.

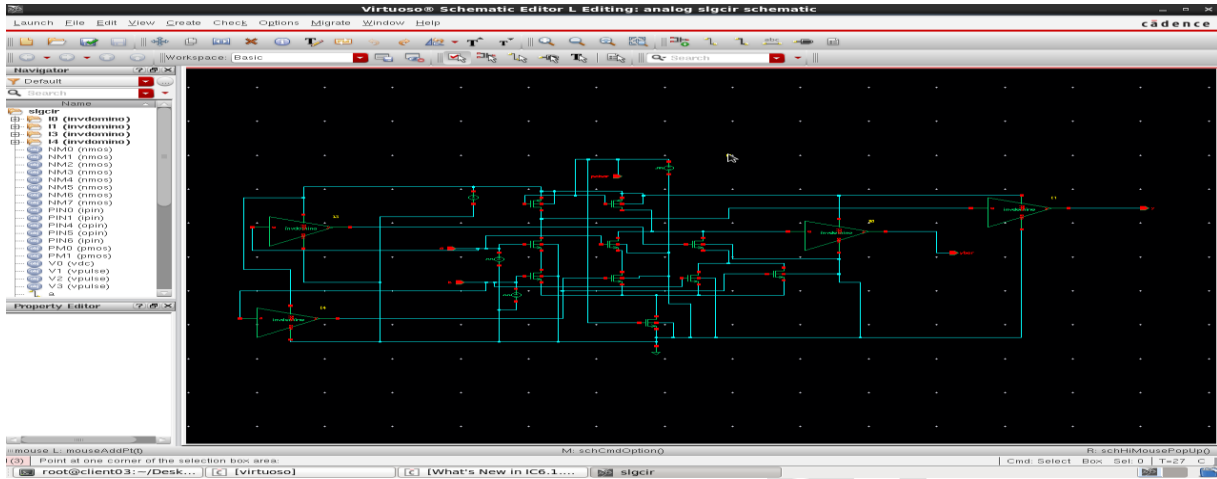


Fig. 2 Synchronizing AND gate

2) *SLGL*: The synchronizing logic gates with a latch function (SLGL) can be extended based on the features of SLG. Fig. 3 shows synchronizing AND gate with a latch function and the table of latch states. The principle is that SLGLs cannot start evaluation without the presence of the enable signal.

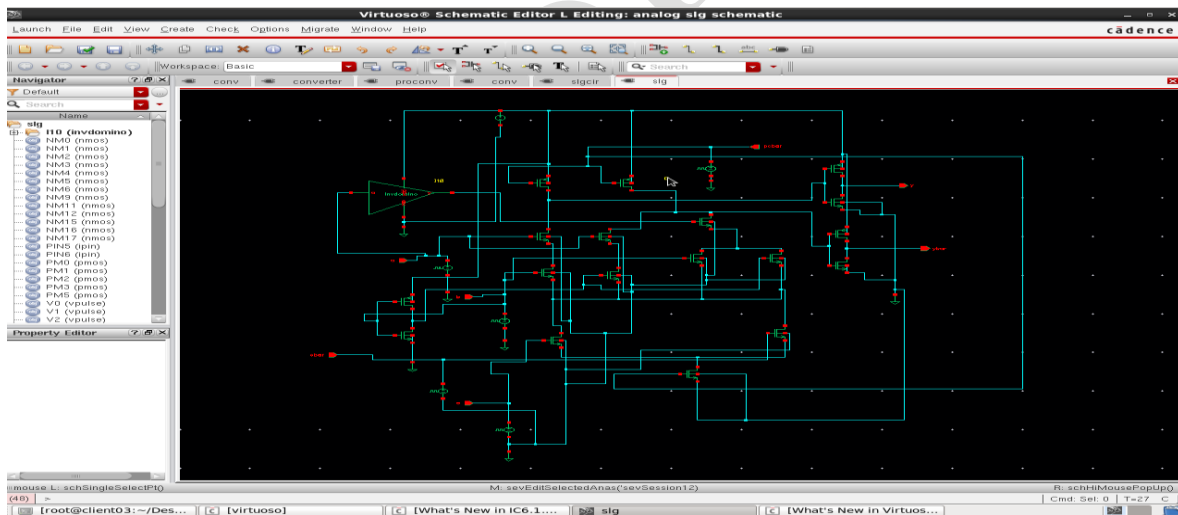


Fig. 3 Synchronizing AND gate with a latch function

3) *S to D converter*: In order to avoid the data transfer error, the encoding converters (Single-rail to Dual-rail) are used with a timing assumption. The encoding converters act as bridge the connection between single-rail domino gate and dual-rail domino gate. Since the completion detector detects only the constructed critical data path, the non-critical data paths do not have to transfer encoded handshake signal. The logic overhead in the noncritical data paths can be reduced by using single-rail domino gates instead of dual-rail domino gates.



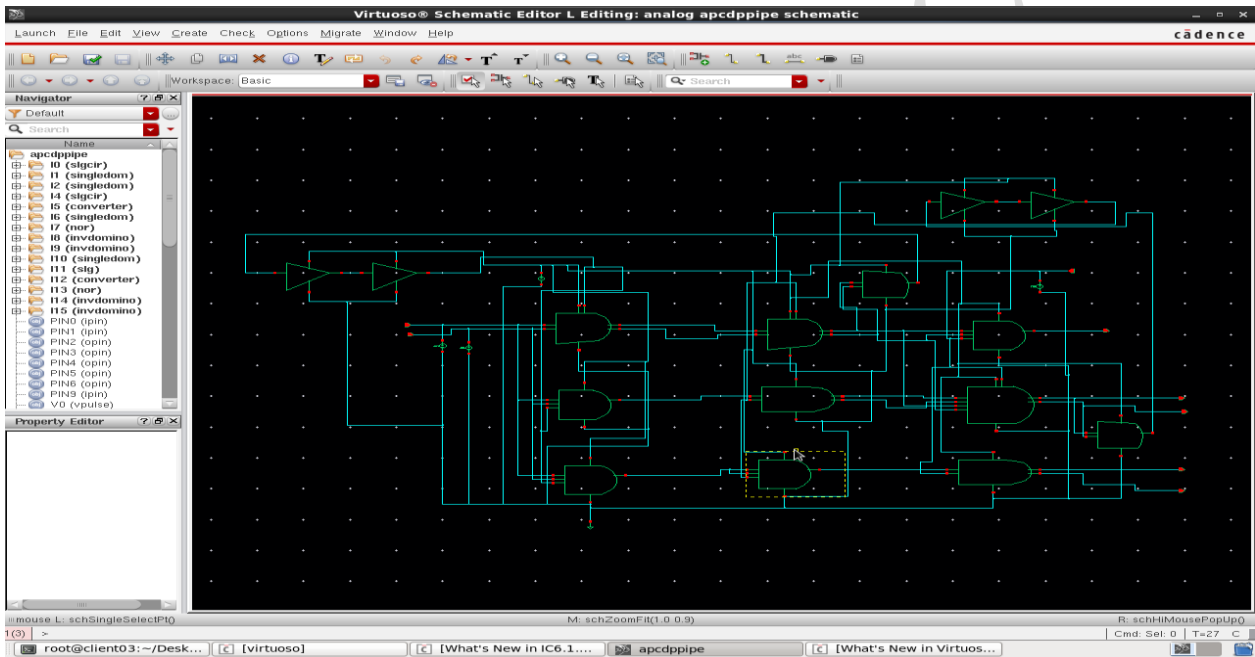
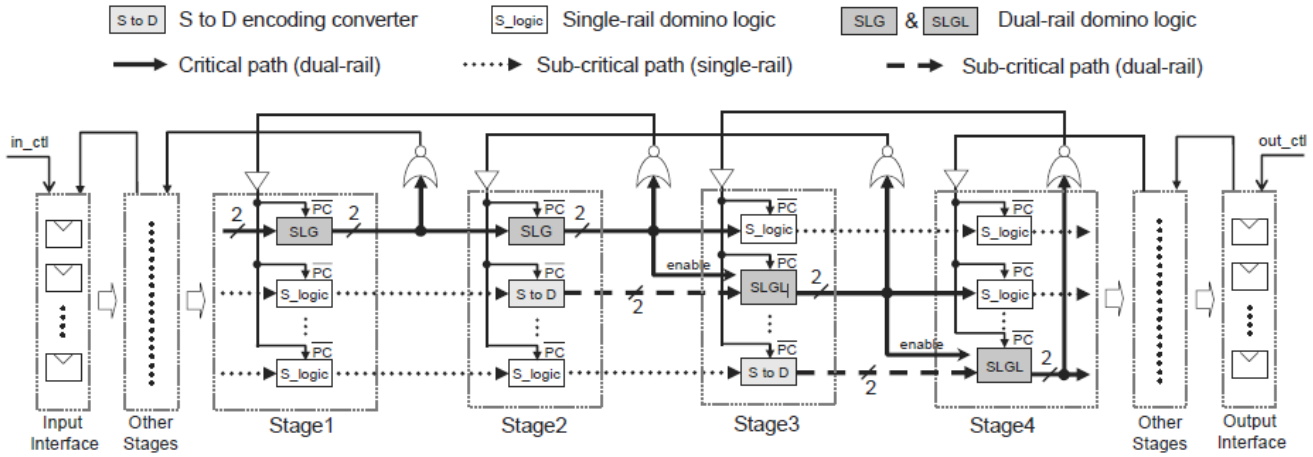


Fig. 6 Structure of APCDP pipeline

### C. EXPERIMENTAL RESULTS

The APCDP pipeline is designed by cadence tool using virtuoso schematic, and the simulation result of this pipeline is showed. The power of the APCDP pipeline can be analysed by using the power calculator and the result will be showed below.

Cadence is an Electronic Design Automation (EDA) environment which allows different applications and tools to integrate into a single framework thus allowing supporting all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies.

Firstly a schematic view of the circuit is created using the Cadence Composer Schematic Editor. Alternatively, a text net list input can be employed. Then, the circuit is simulated using the Cadence Affirm analog simulation environment.



Fig. 7 Simulation waveform of APCDP pipeline

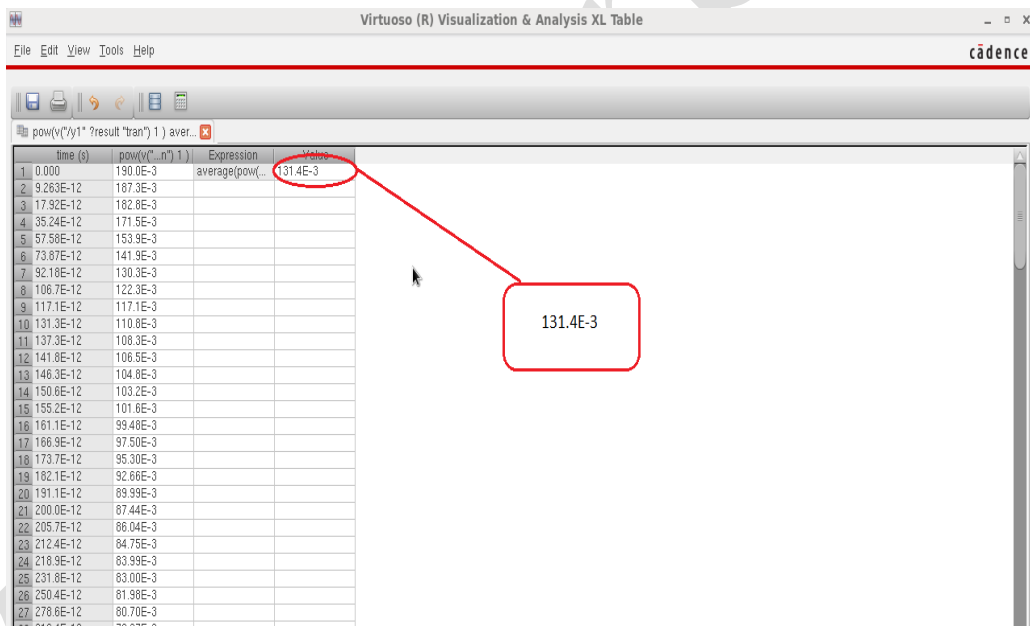


Fig.8 Average power of APCDP pipeline

### III. CONCLUSION AND FUTURE WORK

#### A. CONCLUSION

The asynchronous pipeline can be designed based on the constructed critical data path using domino logic gate, the data path is composed of dual rail and single rail. The dual rail logic is applied at critical data path and single rail is applied at non-critical data path. The design method reduces the handshake control logic as well as function block logic. This asynchronous domino logic pipeline based on constructed critical data path (APCDP) provides lower power consumption,

reduced silicon area, and minimized transistor count. The high-throughput and ultralow-power asynchronous pipeline (APCDP) was designed with the mixer of dual rail and single rail domino logic gates.

## B. FUTUREWORK

The asynchronous domino logic pipeline based on constructed critical data path can be evaluated by using the radix-2 multiplier. Then the evaluated result can be compared with other pipeline techniques such as bundled data asynchronous domino logic pipeline and synchronous pipeline with clock gating.

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